Installation & Operation Manual

Falcon II

cPCI Frequency Reference

S/O/106280C

Table of Contents

SECTION ONE

Introduction

Overview

The DATUM Falcon II serves as a high accuracy clock for the Abis interface cards (AIC) installed in the Datum WARP. Housed in a 6U high and 2 slot wide Compact PCI chassis, the Falcon II is comprised of a precision oscillator frequency source and multiple frequency output circuitry, and a FPGA controller. It provides 2.048MHz and/or 8KPPS TTL output frequencies.

Applications include cellular BTS and LAN/WAN network computers, terminals, routers, switches and computing networks. Falcon II provides the necessary frequency requirements for both CDMA cellular and PCS systems. It will provide a low temperature coefficient and excellent frequency stability without a need for GPS discplining.

The Falcon II is designed for very long operating periods without maintenance. The design will provide a stable frequency with a good short and long term stability, and excellent spur performance. The Falcon II also provides LED status and fault indicators. These status indicators monitor outputs and basic physics operation to indicate when output frequency is outside roughly ±5E - 8 of absolute frequency offset.

Electrical Specifications

- **Output/Frequency/Waveform:** 2.048 MHz & 8 kPPS Differential TTL
  or 1.544 MHz & 8 kPPS Differential TTL

- **Connectors:** cPCI compatible per CompactPCI Spec PICMG 2.0 (Rev. 2.1 sections 2.2, 5.1 and 5.3-7)
  Up to four 9 pin D frequency/sync outputs
  Transition panel frequency/sync outputs
  H.110 CT bus frequency/sync outputs

- **Jitter & Wander:** Meets ITU G.811 and C.812 requirements.
  Meets ANSI T1.101 requirements as a Stratum 2 clock.

- **Aging:**

	OCXO	Rb
Daily:	<2E-10	<2E-10/month
Yearly:	1.2E-8	<1E-9/year
After 20 years:	N/A	<5E-8

- **Frequency Accuracy:** <5E-8 (Rb oscillator - lifetime)

- **Short Term Stability:** (Allan Variance)

	OCXO	Rb
t=1 sec	<3E-11	<3E-11
t=10 sec	<1E-11	<1E-11
t=100 sec	<3E-12	<3E-12

- **Factory Setting:**

	OCXO	Rb
Resolution:	±2 PPM	±2 PPM (±3E-7) range

- **Frequency Accuracy at Shipment:** <5E-11 traceable to NIST

- **Warm-up:**

	OCXO	Rb
Time to Lock:	< 10 min	< 8 min
Time to <4E-10:	<15 min	<12 min

- **Input Voltage Range:** 5 Vdc, 12Vdc cPCI

- **Input Power, Warm up:** 25W

- **Input Power, Normal:** 15W

- **Power quality:** Per EN 61000-4-11

- **Status Monitor:** 4 LED Indicators
  cPCI bus STATUS/CONTROL registers

Note: Consult factory for specifications of oversized oscillator version.

Environmental Specifications

- **Operating Temperature:** 0°C to +45°C ambient

- **Storage Temperature:** -55°C to +85°C

- **Altitude:**

Operating:	-200 ft to 40,000 ft.
Non-operating:	-200 ft to 70,000 ft.

- **Magnetic Field Sensitivity:** ±4E-11 Gauss

- **Relative Humidity:** (operating) 5% to 95%
- **Relative Humidity:** (non-operating) 10% to 95% non-condensing

- **Earthquake:** per GR-63-CORE Figure 5-15, ZONE 4

- **Mechanical:** ETSI Standard ETS 300 019-1-2 Class 2.3 Transportation
  or
  IEC Standard IEC 721-3-2
  ETSI Standard ETS 300 019-1-3 Class 3.2 Operational
  ETSI Standard ETS 300 019-1-1 Class 1.2 Storage

- **EMI:**
  Designed to meet FCC Article 47, Part 15 Class B (conducted and radiated emisions) and EN55011A emissions (radiated and conducted) and EN50082-1 (immunity) when used with shielded intercannection cable.

- **MTBF:**

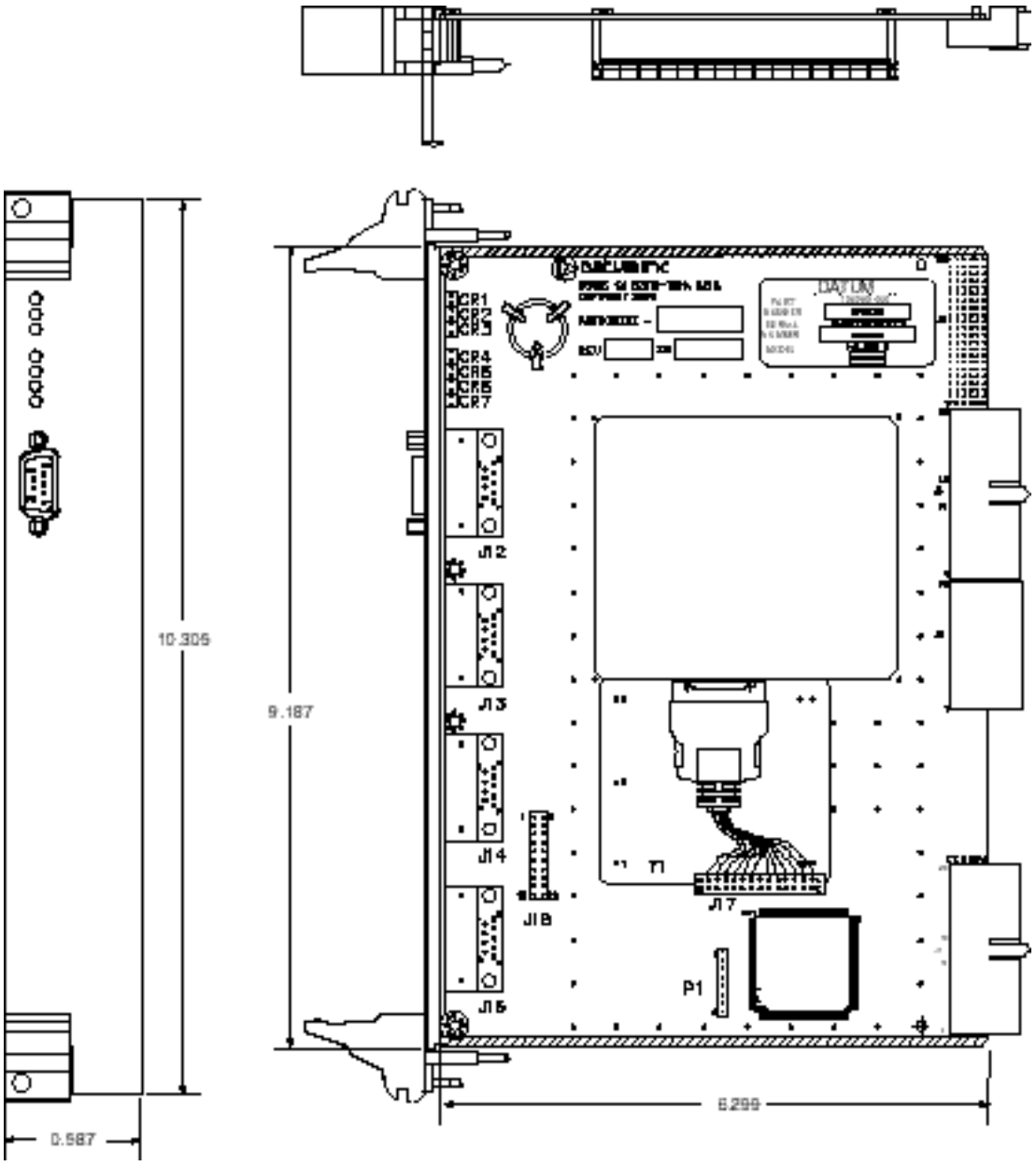
Amb. Temp:	40°C
MTBF (hrs)	greater than 100,000 hours (Bellcore, TR-NWT-000332)

Physical Specifications

- **Weight:** X.XX oz. max.
- **Size:** 6U high & 2 slots wide
- **Warranty:** 1 year
- **Extended Warranty:** Consult factory

Note: Consult factory for application support, test reports or special requirements.

Technical specifications subject to change without notice.



MECHANICAL OUTLINE AND DIMENSIONS

SECTION TWO

Installation

2.1 Setting up the Falcon II unit

2.1.1 Unpacking the unit

Use proper ESD precautions when unpacking the unit. It is shipped in a static protected bag inside a foam container. Check the unit for damage. If damage is found, examine the shipping container. Contact the shipper if the unit appears to have been damaged during shipment. Do not discard the shipping carton until the shipper has an opportunity to make an examination.

2.1.2 Checking contents

Compare the contents of the shipping carton against your sales order and the shipping invoice to make sure you have recieved a complete shipment. If you find a shortage, contact Datum Irvine Sales Department. Have your sales order number available.

If the unit is undamaged and as ordered, you are ready to begin installation.

2.2 Mounting The Falcon II unit in the Chassis

The Falcon II is rack mountable in a standard compact PCI (cPCI) chassis.

NOTE: The Falcon II unit supports hot insertion and extraction. Hot swap compliant staged pins allow unit insertion or extraction from a powered cPCI backplane without damage to the Falcon II or other installed boards or components.

Refer to the Compact PCI Hot Swap Specification for additional information.

Make sure that the extractor handle is in the “remove” position (if it is in the “latched” position the module will not seat properly).

Slide the unit onto the card guide and firmly push it back into the chassis until connector P1 at the rear of the unit seats in the backplane. Once the module has seated move the red portion of the extractor handle to the “latched” position to lock it into place.

Power to the Falcon II is provided through the cPCI backplane connectors. Once it is seated in the backplane, the unit will be powered and the green POWER LED on the front panel will light.

2.3 Connecting cables to the Falcon II Unit

The unit has one DB9 connector (port 1) on its front panel (refer to Figure 2-1) that provides a 2.048 Mhz clock output and a 8 kPPS framesync output. There is a PORT FAULT LED that will light (RED) if an output fault is detected.

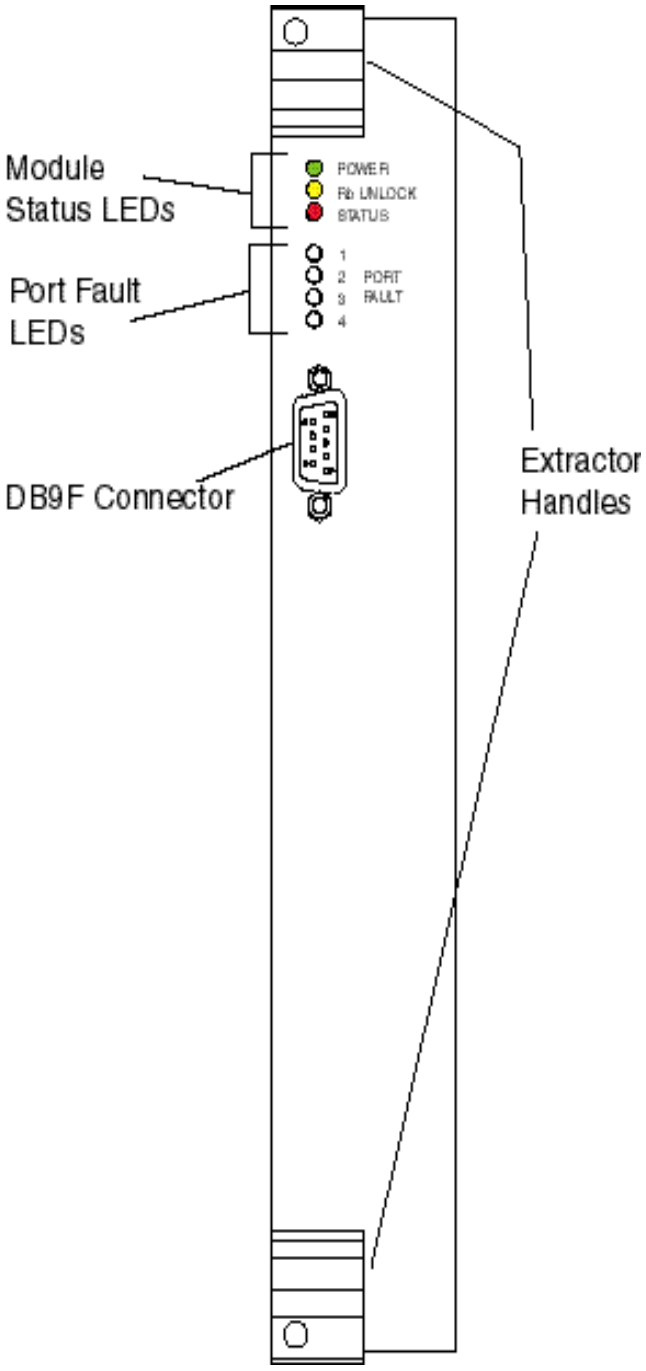
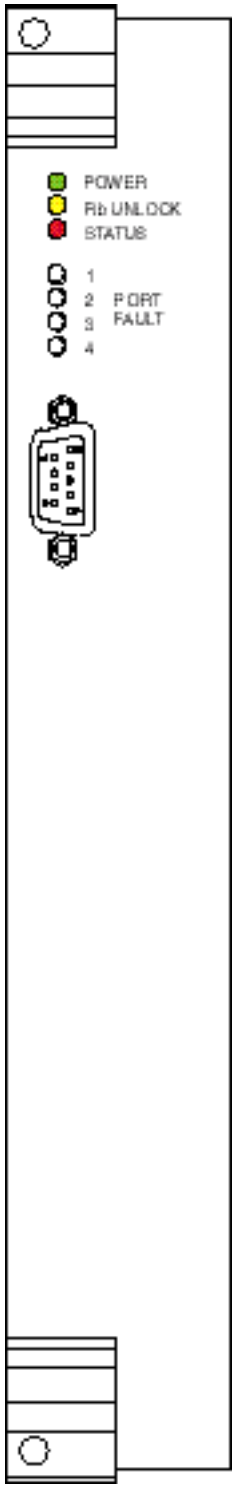


Figure 2-1. Cable Connections and Front Panel LEDs of the Falcon II

2.4 Unit Start-up

Once power is applied all outputs become available within seconds. The unit provides alarm/status indications on the cPCI bus to indicate the unit is in warm-up mode and that the Rb oscillator has not yet locked.



When power is first applied the front panel LEDs will all light to show that they are working. After a few seconds the LEDs will begin to show indications for Falcon II status at that moment.

NOTE: during start-up of a cold unit the Port Fault LEDs will go ON and OFF in a slow sequence that follows system monitoring of the crystal voltage. A unit that is already warmed up may lock right away, and the LEDs will go dark.

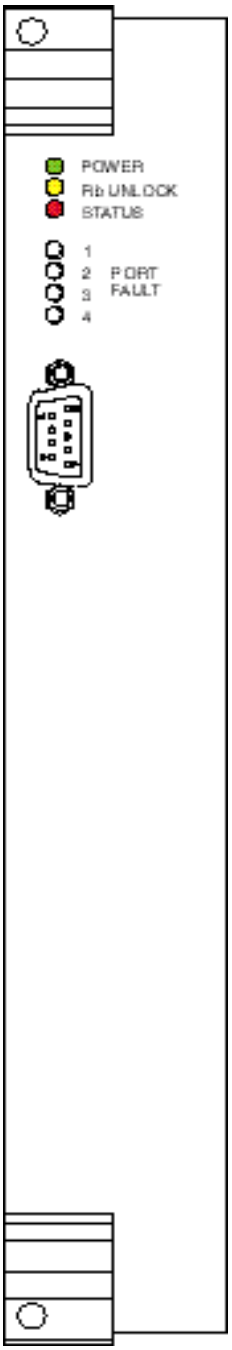
Within a period of 6 to 20 minutes the rubidium oscillator completes the warm-up cycle and achieves lock. An alarm/status message is made available to an external PC indicating this and the yellow Rb UNLOCK LED on the front panel will go dark.

The Falcon II unit is now running in rubidium oscillator disciplined mode and is operational.

2.5 Normal System Operation

The Falcon II operates automatically once the rubidium oscillator has locked and is providing a stable reference clock output.

2.6 System Failure



If the Falcon II experiences a fault condition while operating, the red front panel LED for the failed port will light. If the failure is an oscillator fault, all red PORT FAULT LEDs will light and the yellow RB UNLOCK LED on the front panel will light also.

If the failure is related to a malfunction in the power circuitry, the Green POWER LED will go dark. In this situation the board will still have power.

The red STATUS LED is controlled by the system level software and its state is driven by a register on the cPCI bus.

2.7 Register Interface and LED Activity

The following sections describe in detail the operation of the register interface of the Falcon II.

The register interface consists of two 32-bit register locations in the PCI memory space. The PCI Plug and Play configuration process reports the base address location for these two registers in the PCI Configuration Space Base Register 0. A total of 16 bytes will be allocated to the card, but only the first two 32 bit locations are defined.

2.7.1 Status/Activity Register

The Status/Activity Register is at offset address 0. This register is read-only, and writing to this register will have no effect. If a momentary error occurs for any of the status or activity inputs, the error condition will be latched into the register until it is read. After the register is read, all of the momentary errors are cleared by setting the bits to H (high). If a continuous error is present, the corresponding bit(s) will be held in the low state.

2.7.2 Status/Activity Bit List

This register is designed so that when the board is operating correctly, the lower 16 bits are read as 0xFFFF. The upper 16 bits are undefined, and the lower 16 bits are defined as shown in Table 1.

Table 1 Status/Activity Register

Bit	Name	Write	Read	Set @ Read	Normal State	Notes
00	PowerGood	N	Y	Y	H	H = DC/DC Power Good
01	Lamp_OK	N	Y	Y	H	H = Rubidium Lamp Voltage OK
02	XTAL_OK	N	Y	Y	H	H = Rubidium XTAL OK
03	10MHz_OK	N	Y	Y	H	H = Rubidium Active
04	RbLocked	N	Y	Y	H	H = Rubidium Oscillator Locked
05	16MHz_OK	N	Y	Y	H	H = OCXO Active
06	PLL_Lock	N	Y	Y	H	H = PLL Locked
07	Spare	N	Y	Y	H	Always H
08	8KHz1_OK	N	Y	Y	H	H = Port 1 Sync Active
09	8KHz2_OK	N	Y	Y	H	H = Port 2 Sync Active
10	8KHz3_OK	N	Y	Y	H	H = Port 3 Sync Active
11	8KHz4_OK	N	Y	Y	H	H = Port 4 Sync Active
12	2MHz1_OK	N	Y	Y	H	H = Port 1 2MHz Active
13	2MHz2_OK	N	Y	Y	H	H = Port 2 2MHz Active
14	2MHz3_OK	N	Y	Y	H	H = Port 3 2MHz Active
15	2MHz4_OK	N	Y	Y	H	H = Port 4 2MHz Active
16-31	Not Used	N/A	N/A	N/A	N/A	Reserved – undefined on read

2.7.3 Status/Activity Bit Descriptions

Power Good: A voltage comparator circuit on the board is used to monitor the output voltage of the DC/DC converters. If the voltage is outside of the range required by the X72, this signal will be low.

Lamp_OK: The X72 has an output signal for monitoring the Lamp voltage. A voltage comparator circuit on the board monitors the lamp voltage. This signal goes low if the Lamp voltage is outside of the normal range.

XTAL_OK: The X72 has an output signal for monitoring the XTAL voltage. A voltage comparator circuit on the board monitors the XTAL voltage. This signal goes low if the XTAL voltage is outside of the normal range.

10MHz_OK: An activity detector in the FPGA monitors the amplitude of the 10 MHz sine wave output of the X72 (refer to Figure 3-1). The PCI bus 32 MHz clock is divided down to provide the activity detector clock. If the output amplitude of the X72 changes, this signal will go low.

RbLocked: The X72 has a logic output that indicates the atomic lock state of the Rubidium oscillator. If the oscillator is not locked, this signal will go low.

16MHz_OK: An activity detector in the FPGA monitors the on board VCXO output. The PCI bus 32MHz clock is divided down to provide the activity detector clock. If the 16MHz output of the VCXO is stuck high or low the signal will go low.

PLL_Lock: The board has a PLL to phase lock the VCXO output to the X72 output. The on board PLL circuit has a logic output to indicate the lock state. If the PLL is not locked this signal will go low.

8KPPS_OK: Four activity detectors in the FPGA monitor the Sync signal outputs from Ports 1- 4. The PCI bus 32MHz clock is divided down to provide the activity detector clock. If the Sync output of a given port becomes inactive the signal will go low.

2MHz_OK: Four activity detectors in the FPGA monitor the Frequency signal outputs from Ports 1-4. The PCI bus 32MHz clock is divided down to provide the activity detector clock. If the Frequency output of a given port becomes inactive the signal will go low.

2.7.4 Control Register

The Control Register is located at offset address 4. This register is read/write, and the lower 8 bits are defined as shown in Table 2. The register will power up into the default state shown. The four Fault LEDs, the User LED (for future use) and the Alarm LED are not forced on while in the default state. By default, the output differential drivers and the output activity test receivers are enabled. The upper 24 bits are implemented as a read back register, and do not affect operation of the board. These upper 24 bits can be used by the application software to test the PCI bus signals on the board. Under normal conditions the state of this register should be 0x00000000. The state of these register bits can be read back at the same offset location.

Table 2 Control Register

Bit	Name	Write	Read	Set @ Read	Default	Notes
00	FaultLED1	Y	Y	N	L	H = Force Fault LED 1 On
01	FaultLED2	Y	Y	N	L	H = Force Fault LED 2 On
02	FaultLED3	Y	Y	N	L	H = Force Fault LED 3 On
03	FaultLED4	Y	Y	N	L	H = Force Fault LED 4 On
04	User_LED	Y	Y	N	L	H = Force User LED On (LED CR8 not used)
05	Status_LED	Y	Y	N	L	H = Status LED On
06	Rec_Enable-	Y	Y	N	L	L = Enable Activity Detect Receivers
07	Out_Enable-	Y	Y	N	L	L = Enable Sync/2MHz Transmitters
08-31	Readback	Y	Y	N	0x000	Readback registers for PCI data bus test

2.7.5 PCI Configuration Space Registers

The PCI Configuration Space pre-defined registers will be in the state shown in Table 3. The PCI Plug and Play process defines all of the other PCI Configuration Space registers.

Table 3 PCI Configuration Space Registers

Register	Value	Description
Vendor ID	0x12E2	Datum, Inc.
Device ID	0x2670	Synchronization Support Card
Command	0x0087	I/O and Memory Space, Bus Master, Stepping Control (see below)
Status	0x0400	DEVSEL timing = Slow
Revision ID	0x01	PCI Bus Testability Enhancement
Class Code: Base	0x11	Data Acquisition and Signal Processing
Class Code: Sub-Class	0x80	Other Data Acquisition and Signal Processing
Class Code: Interface	0x00	No Register level interfaces defined
Sub-System Vendor ID	0x12E2	Datum, Inc.
Sub-System Device ID	0x2670	Synchronization Support Card

Due to the design of the Xilinx Spartan PCI core used in the FPGA, the Command Register reports capabilities and requirements that are not used in the device. The FPGA is capable of operating as a Bus Master, but it will operate as a Slave Device. The card does not require I/O space, and the Stepping Control capability is not used.

2.7.6 LED Indicators

The front panel of the Datum Falcon II contains seven LED indicators to show the status of the board. These indicators will indicate faults as listed below. These LEDs are driven by the FPGA to indicate faults based on the signals listed in the Status/Activity Register section above.

2.7.6.1 POWER

This LED shows the state of the Power Good signal from the voltage comparator circuit on the board. It is ON when the DC/DC converter output voltage is within the proper range. It comes ON immediately after power up and stays ON while the board is operating normally.

2.7.6.2 Rb UNLOCK

This LED shows the state of the RbLocked signal from the X72. It will be ON when the X72 oscillator is not locked. It will be ON from the time the board is powered up and will stay ON until the X72 has warmed up.

2.7.6.3 STATUS

Bit 5 of the Control Register is used to turn this LED ON and OFF. When this bit is high, the STATUS LED will be ON. This LED will be in the OFF state at power up.

2.7.6.4 FAULT

A FAULT LED is provided on the front panel for each of the four PORT connectors on the Transition Module. Three conditions can cause one or more of these LEDs to be ON, indicating a fault or functional test.

2.7.6.5 Port Activity Fault

If the activity detector in the FPGA indicates that the Sync or Frequency outputs of a given port are inactive, the LED for that port will light.

2.7.6.6 Internal Fault

If any of the following Status Register bits indicate a fault, all four of the FAULT LEDs will light:

Lamp_OK
XTAL_OK
10MHz_OK
16MHz_OK

During the warm-up sequence while the Rb UNLOCK LED is ON, these FAULT LEDs may momentarily flash ON one or more times.

NOTE: The four FAULT LEDs will not be illuminated if there are faults on the Power Good or Rb Locked signals, since these errors are shown on the POWER and Rb UNLOCK LEDs.

2.7.7 Functional Test

Bits 0 – 3 of the Control Register can be used to force the LEDs ON for functional test. If the corresponding bit is set high, the LED will be forced ON even if no error condition is present.

2.8 Troubleshooting & Maintenance

There are no user servicable parts in the Falcon II. If a major oscillator fault is indicated, return the unit to the factory in it's original shipping container. Call Customer Service for a RMA number and clearly mark this number on the outside of the shipping container.

SECTION THREE

Theory of Operation

3.1 Block Diagram

The Datum rubidium oscillator in the Falcon II generates an accurate, stable, low-noise 10 MHz rf timing output. Status indications derived from the physical operation of the rubidium oscillator can be monitored by the operator through front panel LEDs and status signals sent to the CPU over the cPCI backplane. After a power interruption, the excellent retrace characteristics of the rubidium oscillator enable a fast return to holdover-ready state. The 10 MHz output signal is routed to the disciplining circuitry of the 2.048 MHz and 8 kPPS buffers.

The voltage controlled crystal oscillator maintains a phase locked loop (PLL) while providing 2.048 MHz to the line drivers. Line drivers on each output provide port-to-port isolation while attaining the drive levels required. Output activity detectors on each port allow full self-diagnostics at startup and provide continuous monitoring of signal availability and quality during operation.

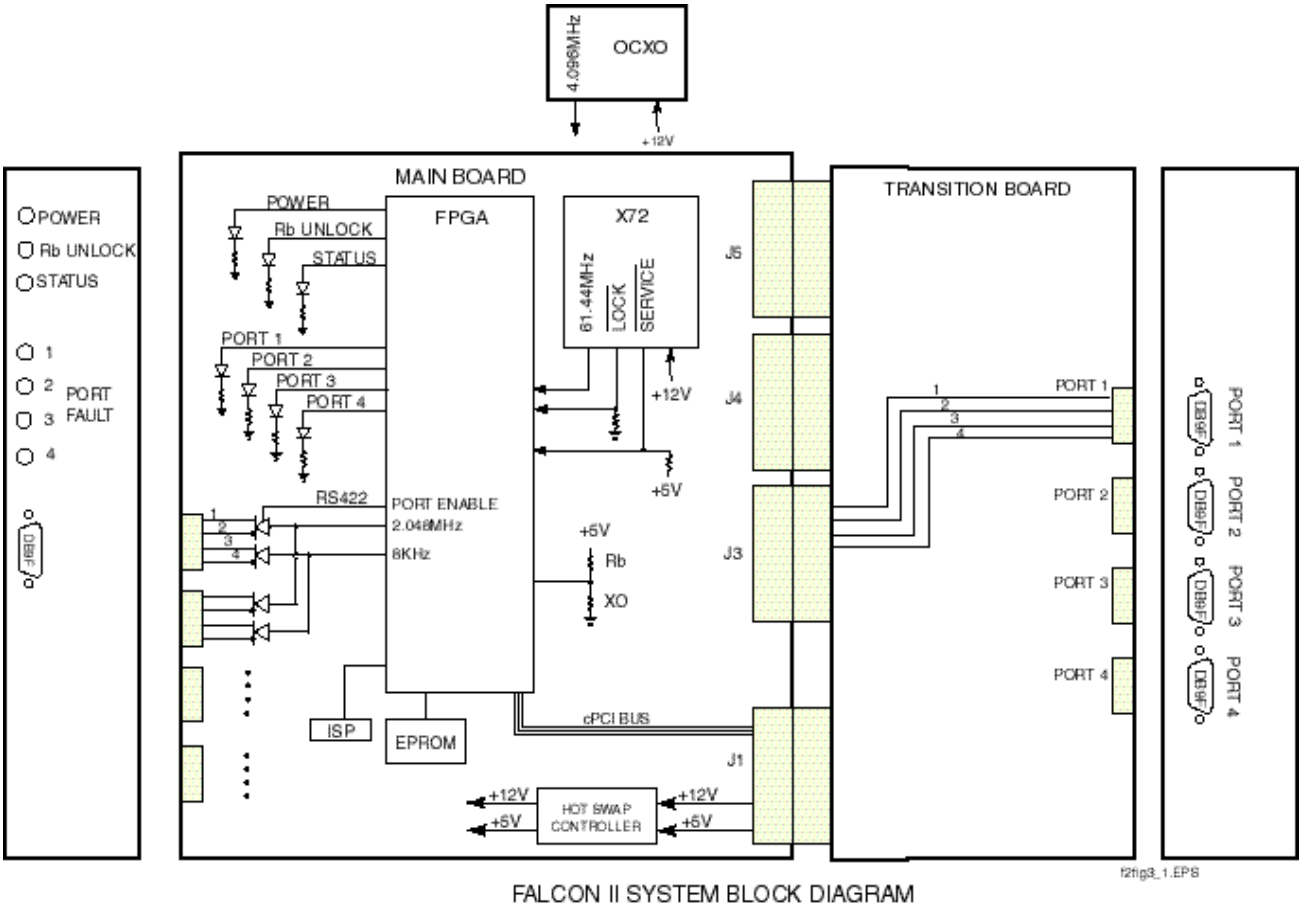


Figure 3-1.

3.2 Theory of Operation

The Datum Falcon II unit contains 2 board assemblies: the front panel board assembly and the main board assembly. Connectors J1 & J6 of front panel board assembly plug into P2 & P5 of the main board and link the circuitry and connectors of the front panel board assembly through the main board assembly to the cPCI backplane.

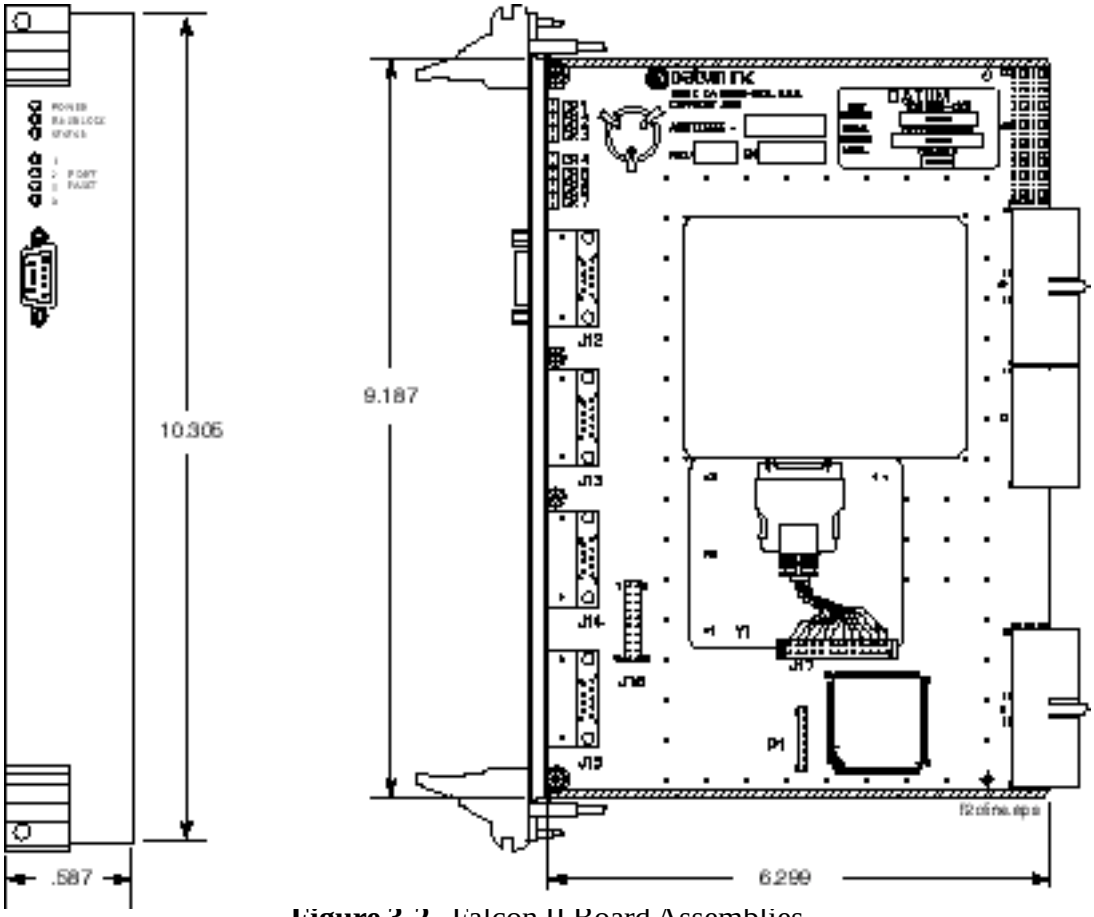


Figure 3-2. Falcon II Board Assemblies

3.2.1 Front Panel Board Assembly

The main function of the front panel board assembly is to buffer and convert the 2.048 MHz signal and 8K PPS signal into differential signals with the RS-422 transceivers (U1-U8). These differential output signals are presented at four 9 pin filtered D-sub connectors (J2 through J5).

The outputs are monitored and these indications are routed through the J1 connector back to the main board for monitoring purposes.

This board assembly also includes 7 LEDs driven by the main board FPGA to indicate the unit status and alarm conditions.

PIN#	SIGNAL/Function
1	EXTSIN/External Frame Sync input
2	No Connection
3	+EXTCK/External Clock input
4	No Connection
5	AGND/Ground
6	-EXTFSIN/External Frame Sync input
7	No Connection
8	-EXTCK/External Clock input
9	No Connection

Figure 3-3. Pin assignments for DB-9 Falcon II output port connector

3.3 Troubleshooting

In addition to the visual indications of the front panel LEDs, the nature of certain output faults can be attributed to failures in specific areas of the main board and display board circuitry.

Display Board Faults

- A loss of a single 8 KPPS/2.048 MHz output.

  Eight individual drivers are used to drive the outputs of all four front panel connectors. If a driver should fail, this will be indicated by the loss of the front panel output driven by that circuit.

Main Board Faults

- A loss of all outputs

  The Xilinx FPGA (U2) on the main board uses the 16.384 MHz output of the voltage controlled crystal oscillator to generate 2.048 MHz and 8 KPPS. A loss of all front panel outputs can be attributed to a failure of the FPGA.

- Outputs gradually drifting off correct frequency