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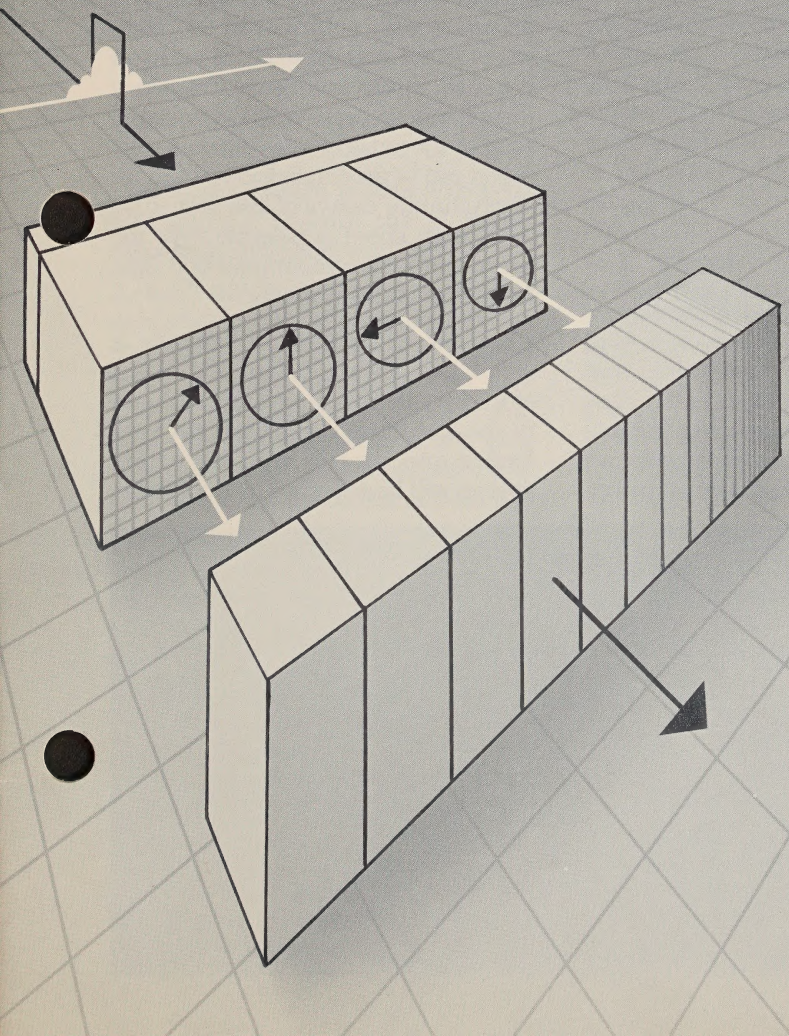
A Rapid-Channel Identifier For EW Receivers



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Tech-notes

This article describes an rf channelizer system designed to improve the intercept probability of a narrow-band receiver. It monitors a wide range of frequencies simultaneously and detects signals in any 1 of 16 bands that are approximately 250 MHz wide. This data is then used to intelligently configure an EW system to maximize intercept probability. Channel detection is accomplished within 15 ns, which permits sorting of frequency data in real time prior to the receiver. The rf circuits are realized in thin film on alumina and can be easily integrated for use in miniature airborne applications.

While designed for a specific application, this rf channelizer has general application in any system requiring real-time sorting of frequency information. This article also describes some of the design trade-offs with a view to other applications.

Introduction

The rapid, accurate, identification of the input signal frequency is a vital parameter for modern electronic warfare (EW) systems. Generally, frequency measurement systems fall into one of two classes. The first employs broadband techniques to simultaneously cover all frequencies. This maintains a high probability of intercept at the expense of possible overload in dense multiple-signal environments. The second class uses narrow-band receivers that are swept in some way to cover a broad range. This trades off probability-of-intercept for the ability to filter out certain signals in dense environments.

The channelizer is essentially a scaled-down instantaneous frequency meter (IFM) and is designed to replace a more conventional multiplexer/detector arrangement (see Figure 1). Two parallel phase discriminators are needed to provide the resolution and accuracy with sufficient phase tolerance for high measurement integrity in dense signal environments. Frequency identification occurs at the very beginning of the pulse because the low resolution can be accomplished with phase discriminator delays of less than 1 ns. Also, high speed is possible with the use of fast ECL comparators and logic in the rest of the system.

Since the channelizer is basically a small, fast, low-resolution IFM, much of the operational theory may be found in the literature [1], [2]. Only the very basics and details specific to this system will be described in this article.

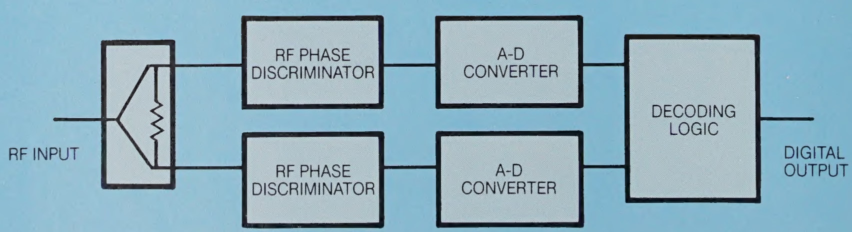


Figure 1. Block diagram of the rf channelizer.

Phase Discriminators

The circuit of a simple rf discriminator is shown in Figure 2. The rf signal at the input is split into two paths, with one path being delayed by a fixed time period. The signals are then fed to a phase comparator made from a 90° coupler and two square-law detectors. Since the time delay is independent of frequency and the phase comparator produces a voltage proportional to the phase difference between the two signals, the circuit operation may be summarized as:

$$RF_{IN} = A\cos(\omega t) \quad (1)$$

RF_{IN} varies in time (t) at the radian frequency (ω).

$$V_{OUT} \propto \frac{A^2}{2}\cos(\omega T) \quad (2)$$

where, T is the rf time delay, i.e., Length/Phase Velocity.

The output voltage is thus a dc level proportional to both the rf signal amplitude and frequency.

A more practical discriminator that uses a balanced configuration is shown in Figure 3. It employs the same principles as in Figure 2, but uses two phase-comparator circuits fed by signals that are 90-degrees apart. This results in two dc outputs of the form of equation (2), one proportional to $\sin(\omega T)$ and the other proportional to $\cos(\omega T)$. The use of these two signals can best be illustrated by considering a polar display such as shown in Figure 4. A single rf signal produces two voltages, X and Y, from the discriminator, and these are fed to the X and Y plates of the oscilloscope. When the rf signal is swept in frequency, with constant amplitude, the display produces a circular trace. The rate of angular rotation is proportional to the frequency change and the delay-line length. Figure 4 ilustrates a useful special case, where the delay line is adjusted to give one complete rotation on the display for a given frequency range (F1 to F2). In this case, the display shows, in polar form, the frequency of any signal in the band. Note also that radial displacement is a measure of the signal amplitude.

A photograph of the rf side of the prototype channelizer is shown in Figure 5. There are two discriminators with associated delay lines and an input power divider. The components of the block diagram (Figure 3) can be easily identified on the photograph. The prototype was made using a modular construction method [3], which is ideal for initial circuit evaluation, but tends to be larger than necessary. Future enhancements to

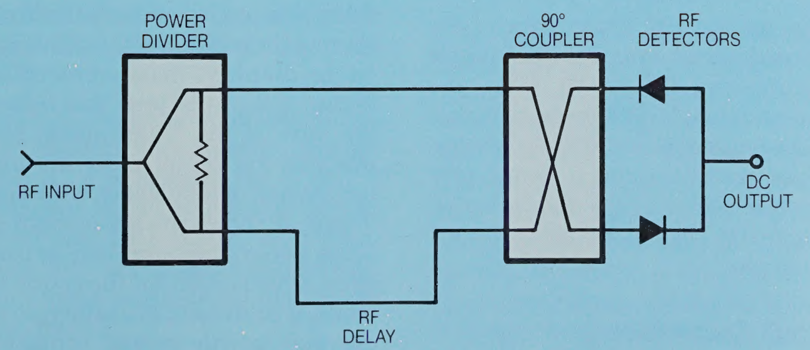


Figure 2. Block diagram of a simple phase discriminator.

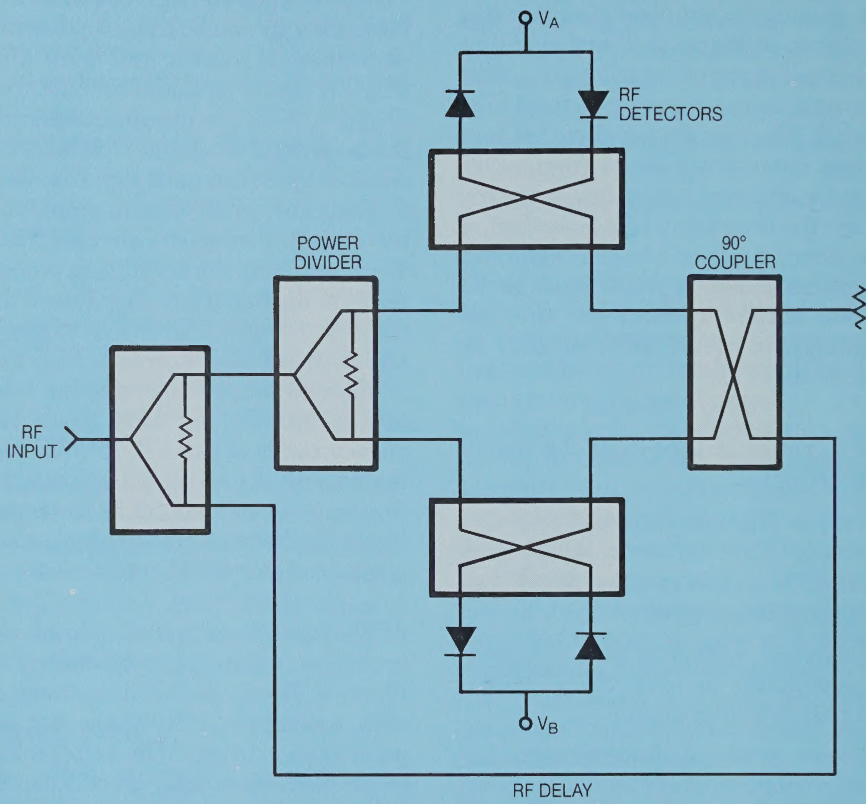


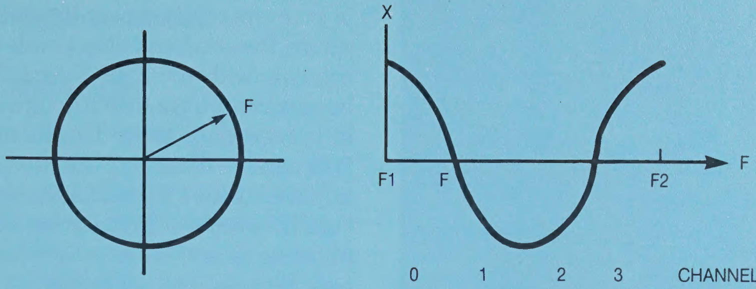
Figure 3. Block diagram of a balanced phase discriminator.

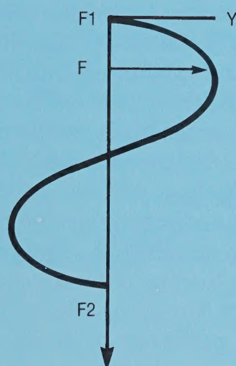
the channelizer technique would reduce the number of individual parts and shrink the size to about 30 percent of that shown.

There are several advantages of the balanced circuit over the more simple discriminator (Figure 2). First, the angular output is linearly proportional to the input frequency. Finally, the two signals produce a unique output over the whole period of the discriminator, compared to just half the period for the simple case.

A-to-D Conversion

The A-to-D converter and decoder represent the most challengining circuits with respect to speed. Very fast ECL comparator circuits are used in a flash A-D configuration. Each comparator is set up as a zero-crossing detector to produce a digital code representing the position of the signal in the polar display. With reference to Figure 4, it can be seen that detecting the zeros of the X-axis signal shows whether the signal is in the top or bottom half of the display, while for the Y axis, it shows the left or right side. Thus, two comparators can be used to show which quadrant the signal is in, which is equivalent to identifying 1 of 4 channels evenly spaced through the band. The amount of angular digitization is referred to as the quantization





CHANNEL	DIGITIZER OUTPUT 0	1	2	3
X	1	0	0	1
Y	1	1	0	0

Figure 4. Polar display and digital encoding of discriminator outputs.

interval and is usually expressed in degrees. Thus, the above method produces 90-degree quantization. Note also, that since the signal amplitude corresponds to the radius on the display, this method is insensitive to signal amplitude variations.

Additional comparator circuits can be used to produce finer degrees of quantization. This is because the X and Y signals are, in fact, orthogonal vectors and so can be summed to produce signals with zero crossing shifted with respect to the originals. Since it can be shown that,

$$K\sin(\omega T) + \cos(\omega T) = P\sin(\omega T + Q) \quad (3)$$

where, P and Q are constants fixed by K:

$$P^2 = 1 + K^2$$
$$Q = \arctan(K) \quad (4)$$

then, combining a weighted sum of the discriminator outputs, $\sin(\omega T)$ and $\cos(\omega T)$, produces a signal of the same form but shifted in phase by a constant determined by the weighting factor. This technique can be applied more than once to generate any degree of quantization; however, in practice, there is a limit due to the accuracy of the discriminators and the multiplicity of circuits required.

The other application for the weighting technique is to adjust the position of the

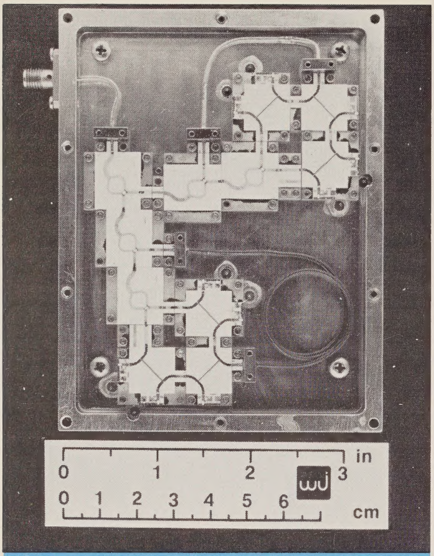


Figure 5. Photograph of the rf circuits in the prototype.

zero crossings so that they correspond to the desired channel break points. Figure 6 shows the actual polar output from the discriminator used in the system. The accuracy of the circuit is evident from the quality of the circle displayed. Note that even though the delay line has been correctly adjusted to give one rotation over the frequency range, the start and stop points do not coincide with the X or Y axis. This is because the phase shift through a cable is proportional to its length and the frequency. Thus, if the length is adjusted to give a specific phase difference between two frequencies, then the absolute phase shift at any one frequency cannot be controlled.

The band-edge phase offset shown in Figure 6 can be corrected by applying the weighting technique to the two discriminator output signals prior to the A-to-D converter. This lines up the edge of the operating band, F1, with the edge of the first channel. The alignment of the other channels, within the system linearity, is then automatic. In practice, the weighting is done by a resistive network on the comparator inputs, and a buffer amplifier is required to minimize the loading of this circuit on the rf detectors. The gain of the buffer is set to provide sufficient over-voltage to the

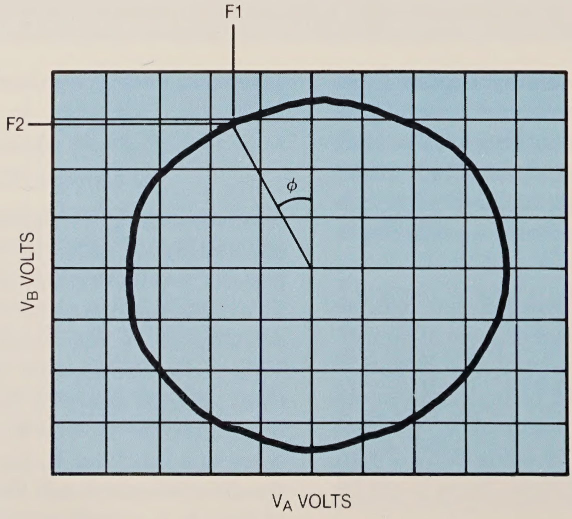


Figure 6. Measured polar display of the prototype discriminator.

comparators for a given rf sensitivity, and the bandwidth must be adequate for the system response time.

Decoding Logic

Practical limitations such as phase and amplitude tracking limit the digitization of each discriminator output to eight channels. Increased resolution is obtained by using several discriminators in parallel with multiple delay-line ratios. The key is to use data from the short delay discriminators to identify the signal frequency in a coarse way, and then use data from the successively longer delay circuits to produce the increased resolution. This is exactly the same as a traditional IFM, except that relatively few discriminators are needed and the resulting system is smaller and faster.

The alignment of two or more discriminators in a system is a complex problem with many contributing factors. However, the simple two-discriminator system designed for this application *does* give some insight into how the system works.

Each discriminator with its A-to-D converter produces a digital output code depending on the rf frequency. Figure 7 shows a truth table for all possible codes where the frequency ranges of the channels are identified by the channel number. Note that the channels are all the same width and are contiguous. The digital output of discriminator #1 (channels A, B, C and D) correspond to the 45-degree quantization of the signal shown in Figure 6. The discriminator #2 output is a similar code, but with half the period because the rf delay cable was adjusted to give two rotations in the band.

Individual channel identification is accomplished by combining the output codes to give a unique logic output for each channel. Using channel 4 as an example, combining the output from channels E and H with a logical AND defines the edges of that channel (see Figure 7). It also has the side effect of identifying a second or ambiguous band (channel 12). This may be resolved by including channel D from discriminator #1 in the AND operation. Similar logic may be applied to all the other channels, resulting in 16 logic comparisons for the entire decoding process. Decoding of each channel may be done in parallel so the whole process takes only one gate delay and could be integrated into a gate array.

	RF CHANNEL																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	DISC #1
B	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	
C	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	
D	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
E	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	DISC #2
F	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	
G	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	
H	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	
E.H.	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	
E.A.D.	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	

Figure 7. Truth table and ambiguity resolution for a two-discriminator system.

System Tolerance

The decoding logic example above shows that the alignment of the edges of outputs E and H are critical in defining the edges of the particular channel, while the exact position of the edge of output D is only secondary. It is generally true that the channel edges are defined by the outputs from discriminator #2, while those of discriminator #1 are only used to resolve the ambiguities associated with the decoding. This principal is important because it allows a degree of tolerance in the discriminator #1 outputs without changing the decoded channel output. In fact, channel D was used in the example because it has the widest margin between its output crossover frequencies and those of channels 4 and 12. It is this margin which provides immunity to noise and simultaneous signals in the system [1].

System Performance

The key elements in system performance may be summarized by considering the accuracy, dynamic range, tolerance to simultaneous signals, and the speed of the channelizer.

The accuracy is a measure of the difference in frequency between the nominal and actual channel break points and is shown in Figure 8, column 2. The system operates over the 2 to 6 GHz range, with a nominal channel width of 250 MHz. Only 12 channels were actually required by the EW receiver, and this is reflected in the results. The remaining 4 bands identified by the channelizer exist in pairs on either side of the operating band and are not used. The accuracy is shown to be within +4.5 to -7.5 MHz.

The dynamic range is measured by adjusting the rf input signal level and

Channel No.	Frequency Accuracy MHz	Simultaneous Sig	
		Lower Edge dB	Upper Edge dB
1			1.9
	-7.5		
2		4.6	4.5
	1.9		
3		3.5	3.7
	-5.0		
4		4.7	4.3
	4.5		
5		4.4	3.8
	-6.5		
6		5.1	5.1
	-6.4		
7		5.6	3.7
	-0.3		
8		4.7	4.9
	-1.0		
9		5.0	3.9
	-7.0		
10		5.5	3.2
	-4.8		
11		4.4	3.2
	-2.5		
12		1.1	

Figure 8. Summary of the prototype system performance.

measuring the accuracy. The channelizer accuracy decreases with reduced power input, but maintains ±10 MHz accuracy for signals in the range of +6 to –4 dBm.

Simultaneous signal performance is also shown in Figure 8. In this case, one signal at a fixed power level and at the edge frequency of a channel is fed into the channelizer with another variable signal. The variable signal power is then increased from a low level and the frequency adjusted until a level is reached where corruption of the digital output code occurs. This difference in power between the two signals is the simultaneous signal tolerance. The results in Figure 8 show a worst case of 5.6-dB tolerance to an interfering signal.

Note that in practice both the dynamic range and simultaneous signal performance may be improved by using limiting rf amplifiers before the channelizer. For example, a typical 6-stage limiting amplifier produces ±3 dB output over an input range of 50 dB. In addition, low-level signals with 6-dB difference in amplitude at the input are compressed such that there is 11-dB difference at the output.

A worst-case measurement of speed was made with the rf frequency at the band edge. The detection speed from 50% input to 50% ECL output was 7.5 ns (see Figure 9). This measurement does not include the single gate delay associated with the decoding logic but, nevertheless, illustrates the rapid speed of the system.

Finally, although temperature stability was not part of the original objectives for this prototype, it has been measured. As would be expected, the accuracy degrades at the extremes of the military temperature range and the accuracy margin expands to ±35 MHz. Estimates show that this degradation is primarily due to changes in the weighting resistor circuits and may be improved by using temperature-compensated components.

Applications

The channelizer has been used as a direct replacement for a multiplexer/detector system. In comparison to the

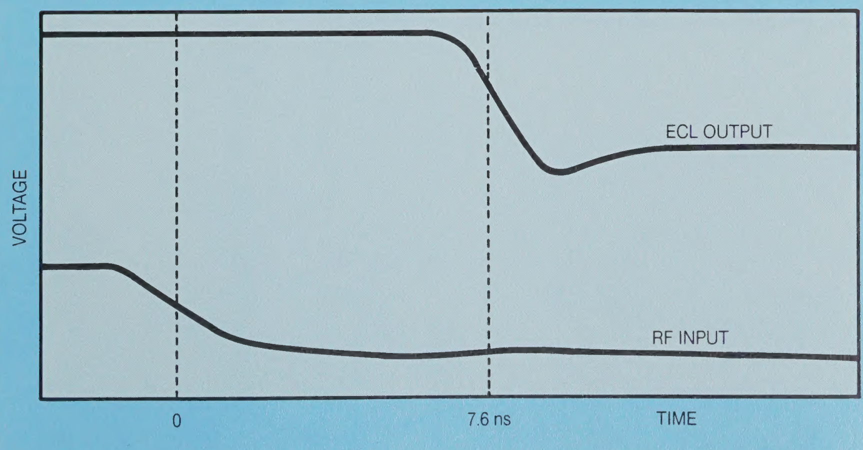


Figure 9. Measured pulse-detection speed of the prototype system.

multiplexer, it is very simple to align and has the potential for faster operation and greater resolution. This is because the major factor in speed for the multiplexer is the filter group delay, which is fixed for a particular channel spacing. In contrast, the channelizer speed is primarily limited by the A-to-D conversion time, and this may be improved using faster logic. Greater resolution is also possible because the rf time delay is very small. For example, if the prototype unit described in this article had double the resolution, that is, 32 channels, the resulting increase in identification time would be less than 5 ns.

The channelizer method also offers great flexibility compared to a multiplexer because the number and widths of the channels do not depend on the design of individual rf filters. The only limit is that all channels have to be either the same or integer multiples of the same width. Within the wide frequency range of a discriminator, the number of channels is determined by the quantization interval, and the channel widths are then set by the shortest delay-line length. Consideration of multiple-signal tolerance involves a trade-off between the number of parallel discriminators and the number of video comparators. In summary, therefore, several different channel number/width designs are possible using the same basic rf and video circuits in different combinations and with particular delay-line lengths.

The first application of this system was for a broadband EW receiver using digital signal processing. The signal processor base bandwidth was limited to approximately 250 MHz, so a front-end downconverter was needed to cover the 2-to-6 GHz band. The channelzier was used to monitor the 4-GHz wide band, detect signal presence and automatically select the correct LO frequency for conversion to the signal-processor baseband. The high speed was required to enable the receiver to respond on a pulse-by-pulse basis.

The prototype channelizer described in this article may have other applications. The key feature is the ability to identify and sort rf signals over a wide frequency range and at bandpass, or bandstop filters in the front end of any receiver system. Also, the ability to identify channel activity has potential for signal switching in systems which employ multiple parallel processors such as Bragg cells or compressive receivers.

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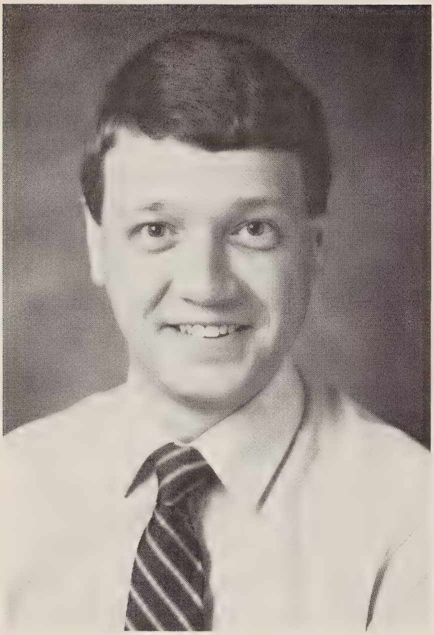
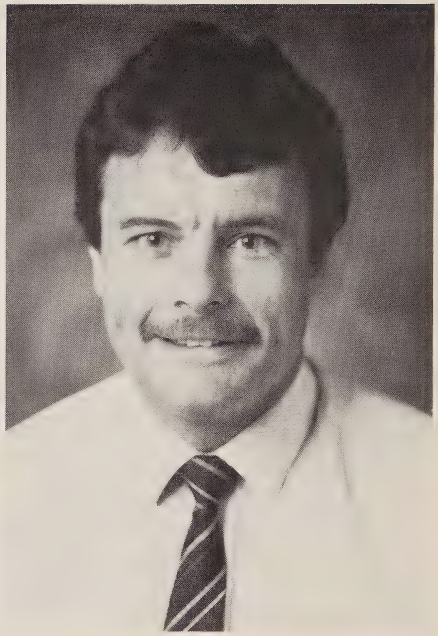




Dr. Richard G. Ranson

As a senior design engineer in the Advanced Subsystems Development Section, Dr. Ranson is responsible for research and development of various on-going department projects. Particular specialties include filters, couplers and switches. The most recent project involved the development of a novel, very high speed channel-identification system based on frequency discriminators.

He has also served as project leader responsible for the development of the microwave front end for a spectrum analyzer. Other work includes circuits for a fast, direct-frequency synthesizer.

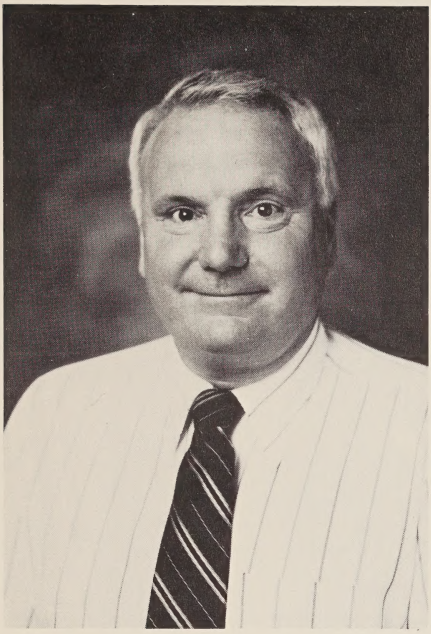
Dr. Ranson holds a B.Sc. from the University of Leeds, England, and a Ph.D. from the University of Leeds, England. He is a member of the IEEE and MTT.

Dr. Gregory L. Hey-Shipton

As Head of the Advanced Subsystems Development Section within the Subsystems Research and Development Department, Dr. Hey-Shipton is responsible for the research, development, and design of new devices and subsystems using GaAs FET devices, amplifiers, doublers, microstrip, stripline, suspended substrate, coplanar waveguide, mixers, filters, switches, couplers, and associated circuitry.

He has been involved in the design of many of the subsystems products currently in production as well as the design of new components. In particular, Dr. Hey-Shipton has developed a range of novel microstrip filters and miniature switched air-cavity filters.

Dr. Hey-Shipton holds a B.Sc. from the University of Manchester, England, and Ph.D. from the University of Leeds, England. He is a member of the Institute of Electrical and Electronic Engineers.



Dr. John G. Galli

As Manager, Subsystems R&D Department, Dr. Galli is responsible for scientific and engineering advances leading to state-of-the-art electronic warfare and radar microwave subsystems. Sustained efforts are underway for device characterization and modeling through 18 GHz, GaAs MMIC design, and microwave component development. Passive and active circuits include silicon and GaAs transistor amplifiers, mixers, samplers, PIN diode limiters and switches, filters and multiplexers. Under his leadership are broad-based programs in the mechanical engineering and materials science fields, dedicated to the development and application of advanced hybrid microwave integrated circuit manufacturing technologies.

For several years he was responsible for development of the AMRAAM RF Processor and, more recently, has been directly involved in successful development of expendable decoy microwave subsystems and a digital rf memory signal processor. All of these programs have relied upon high levels of device integration in hybrid MIC media. More recently, GaAs MMIC integration technology has been employed to meet user requirements.

Dr. Galli also contributed to original research efforts in the Electron Paramagnetic Resonance study of certain metallocene compounds and developed a low-temperature (1.5°K), superheterodyne, X-Band, synchronous detection attachment for the spin resonance spectrometer. He collaborated with a group of Organic Chemists in developing methods for rapid EPR analysis of a short-lived class of free radicals.

Dr. Galli holds a BA in Physics from San Jose State University, and a Ph.D. in Solid State Physics and Electrical Engineering from the University of Idaho.

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