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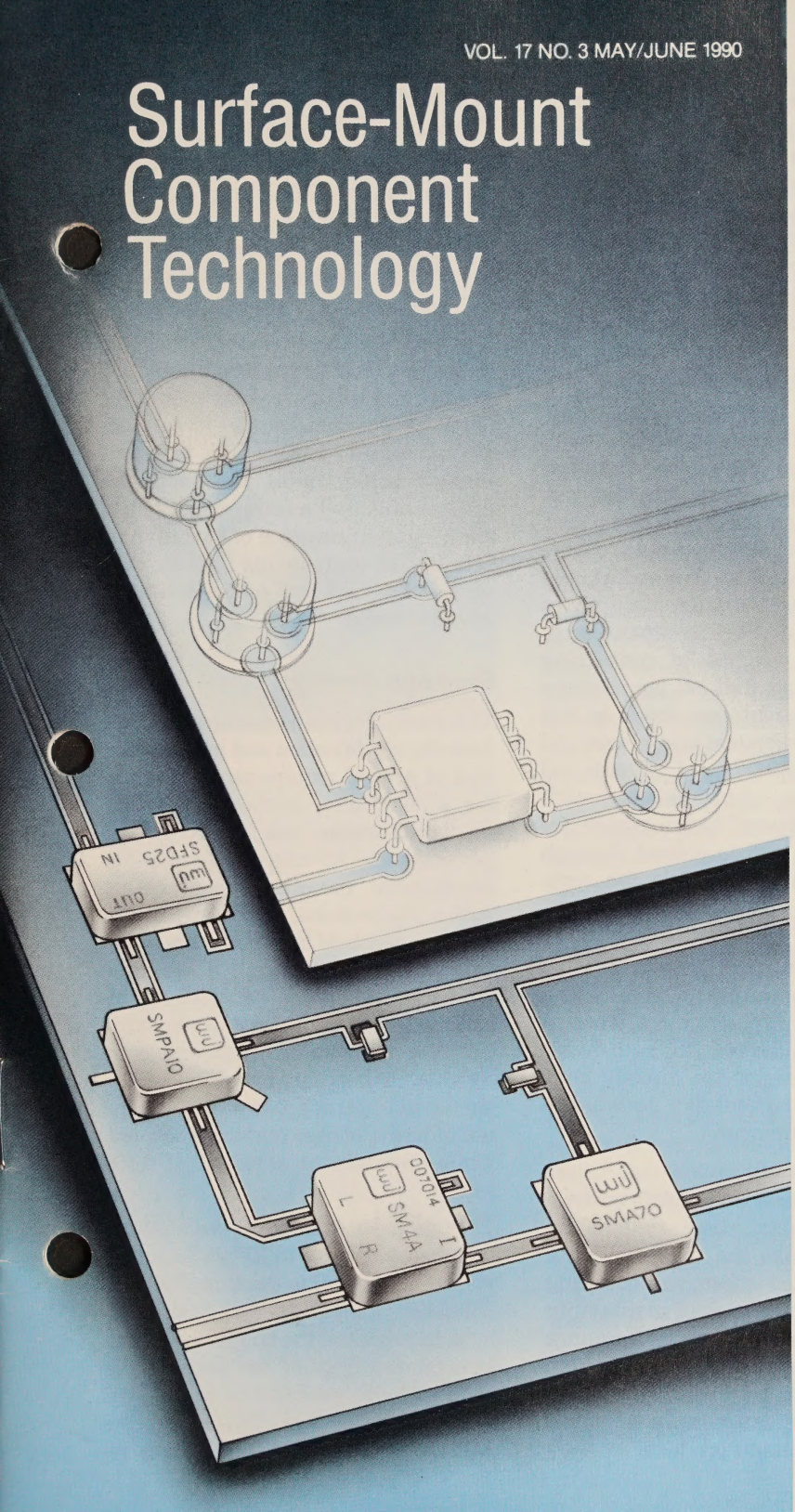
Surface-Mount Component Technology



WATKINS-JOHNSON COMPANY Tech-notes

The emphasis on improving performance by adding new features, while at the same time reducing overall system cost, continues to be an industry trend. Even with the use of MMICs, a large gap still exists when it comes to the RF and microwave hybrid components that are needed to improve system performance. One way to improve these components is to improve the way that they are packaged.

Continuing advances in surface-mount technology have enabled manufacturers to reduce system size and cost. The typical board size can be reduced by as much as 40% by replacing conventional TO-8, TO-5, dual in-line, and flat-pack packages with surface-mount components [1]. Surface-mount technology is a method of connecting components so that all connections to the components are made in one plane. The component is also mounted on this same surface. Conventional packages are often mounted with "through-the-board" technology where the package lead is passed through the board and soldered to the opposite side.

These conventional packages often require elaborate circuit boards and manual assembly techniques, whereas the surface-mounted RF and microwave components are directly compatible with current-day automated-assembly equipment.

Watkins-Johnson Company's surface-mount products allow system designers to make the transition to a surface-mounted system without being hampered by the lack of availability of various products. The performance already experienced by the system designer using conventionally packaged products can now be achieved with surface-mount products.

The surface-mount package advantages are:

- Excellent RF and microwave performance to 7.5 GHz
- High Reliability
- Wide product selection
- Full compatibility with automated assembly techniques.

This article will describe the construction of surface-mount amplifiers and mixers, and will discuss the mounting of these components to a printed-wiring board (PWB). The environmental integrity of the mounted components and a comparison of the electrical performance of several surface-mount components to their conventionally packaged counterparts are also discussed.

Package Concept

The surface-mount packages evolved from the identification and implementation of several requirements essential for a successful surface-mount RF product. Attention was focused on size, performance, structural integrity for mechanical mounting, inspectable solder connections, and hermeticity. The size was held to a minimum, while still accommodating all of Watkins-Johnson Company's RF products, including amplifiers, mixers, attenuators, limiters, frequency doublers, and hybrids. Both surface-mount packages, shown in Figures 1A and B, allow the use of ferrite chokes and transformers, while maintaining a height of 0.160 inches.

The internal-to-external RF feedthrough design has resulted in RF performance virtually identical to existing Watkins-Johnson Company's standard products. In addition, the bonding-pad pattern on the floor of the packages is identical to the pin patterns on the TO-8 header and flat pack. This makes the SMTO-8 and the SMFLAT direct re-

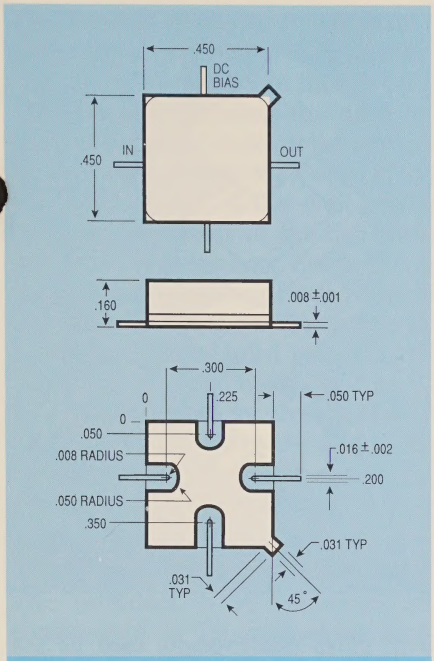


Figure 1A. The SMTO-8 outline drawing.

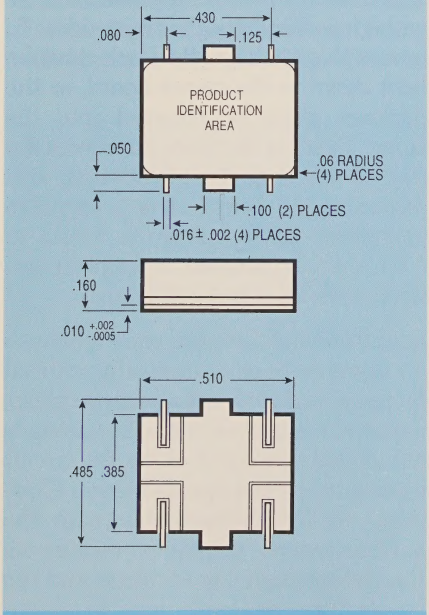


Figure 1B. The SMFLAT outline drawing.

placements for the TO-8 header and the flat pack, respectively. In fact, the exact circuit layout and component orientation found in TO-8 and flat-pack designs may be placed directly into their surface-mount counterparts. This compatibility allows the use of proven manufacturing techniques, thereby maintaining high manufacturing yields.

Package Construction

Although the SMTO-8 package was designed in-house and the SMFLAT package is provided by an outside vendor, both packages share common manufacturing methods. The surface-mount packages utilize a kovar lead-frame, an alumina base, and a kovar seal-ring, respectively (see Figures 2A and B). When the three pieces are brazed together and electrically connected using solid metal vias in the alumina, a mechanically strong, temperature-resistant package is created. Along with mechanical strength, the rectangular outlines make for easier handling by pick-and-place equipment; a great benefit for an automated assembly environment.

The surface-mount package construction also provides improved thermal performance compared with conventional counterparts. The conventional TO-8 package is made from kovar (0.061-inch thick), a material with poor thermal conductivity. However, the SMTO-8 package uses a ceramic base and a kovar (0.008-inch thick) lead-frame that lowers the thermal resistance by 15%.

A high-reliability market requires military specifications for visual criteria on soldered connections. For this reason, the leads on the surface-mount packages protrude 0.050-inch so that the solder fillets may be easily inspected. If visible solder joints are not a requirement, the leads may be sheared flush

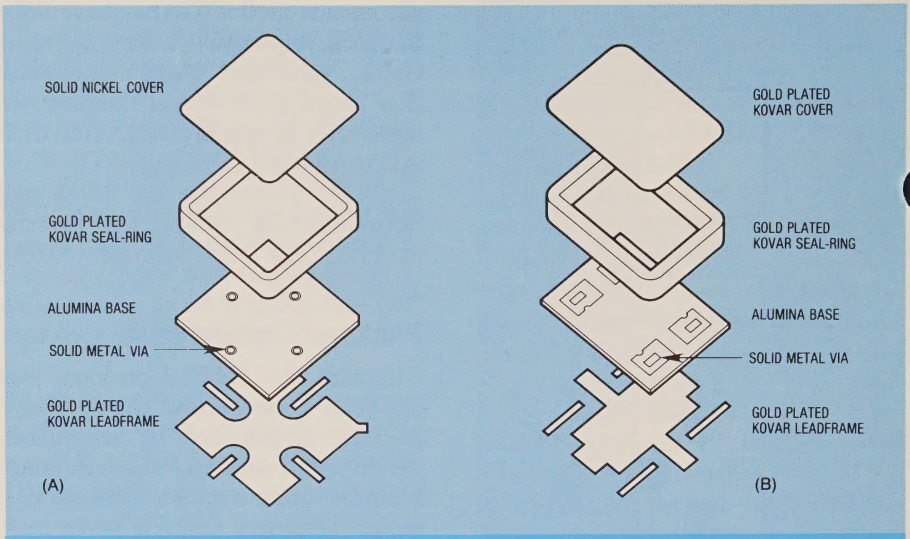


Figure 2. Construction of the SMTO-8 (A) and SMFLAT (B).

with the base of the packages to achieve a greater component density on the board. The thickness of the leadframe along with the channel around each lead (see Figures 1A and B) allows flux to be washed away by using flux removers.

Other major concerns for package compliance with MIL-STD-883 are hermeticity, salt spray, and humidity. Failure in any of these three requirements is quite often associated with damaged glass-to-metal seals. Since the surface-mount packages do not utilize glass-to-metal seals as do other packages, compliance with MIL-STD-883 becomes much more consistent. The cover is parallel-seam sealed to the package, thereby achieving a leak rate of less than 5×10^{-8} atm-cc/s.

Package Comparison

As with most new concepts, the surface-mount packages evolved from their predecessors, the flat pack and the TO-8 package. The TO-8 (0.5-inch diameter) package consists of a kovar header with glass feedthroughs used as the interconnects. The mismatch loss associated with this design allows for operation up to 5.5 GHz with 1-dB insertion loss and 13-dB return loss.

The flat pack is a rectangular package with glass feedthroughs on its sides. To mount this package, the leads must be bent down to the circuit board, or the package must be recessed into the board. Bending the leads introduces the risk of cracking the glass seals, and recessing the board is an expensive operation. This package is useful to 5 GHz when mounted in a test fixture that emulates a recessed board.

Both TO-8 and flat-pack packages have an upper-frequency limitation caused by the shunt capacitance of the glass-to-metal feedthrough and inductance associated with connecting the circuit internally to the feedthroughs. However, the feedthrough design in the surface-mount packages minimizes the feedthrough capacitance, and the bonds from the feedthrough to the circuit are shorter, thus lowering the associated inductance.

The leads of the new surface-mount packages do not extend from the bottom of the package like those of the TO-8, thus eliminating the need for nonplated through-holes in the printed-wiring board. Nor do the leads extend from the middle of the wall of the package, like those of the flat pack; this eliminates the need for recessing the printed-wiring board and/or bending the leads for mounting purposes. These features, coupled with the performance of 1-dB insertion loss at 7.3 GHz (7.6 GHz for the SMFLAT), and 12-dB return loss (13-dB for the SMFLAT) give the system designer a significant advantage.

Package

The introduction of surface-mount components to the engineering community is not a new idea. Surface-mount digital ICs and passive devices have been used for over 10 years. However, the introduction of surface-mount RF components has been more difficult. With increasing frequency, the transmission medium and device interconnections are of greater concern to the electrical engineer, as these can limit the system performance. The mismatch loss between the various interconnections (i.e. the PWB, the package and the device) must be minimized to insure good frequency performance.

Two modeling techniques can be used to determine the useful frequency range of the surface-mount packages. One approach models the device as a combination of series and shunt reactive elements. The construction of the package as illustrated in Figure 3A can be modeled as in Figure 3B. The inductance associated with the via hole (L_{via}) is directly related to the diameter of the via and is a limiting factor in the upper cut-off frequency of the package. As the diameter of the via is increased, the inductance is lowered and the package will exhibit better return loss. However, the diameter is constrained by the size of the overall bonding area and the manufacturability of the part. The substrate capacitance (C_{sub}) models the capacitance between the ground plane inside the package and the lead frame. This parasitic capacitance can be minimized by the use of ground vias located

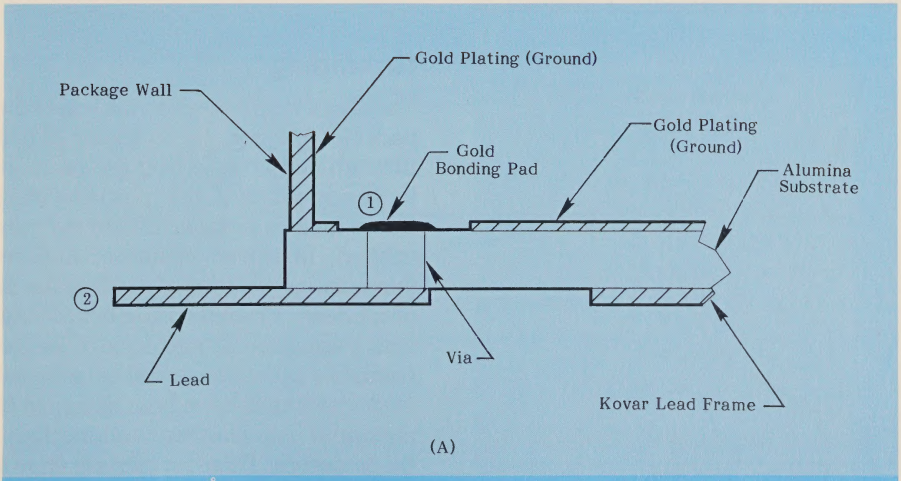


Figure 3A. A cross-section of the SMTO-8 package showing the leadframe, ceramic base, metal via and kovar wall.

as close as possible to the interconnect via. Finally, the lead inductance (L_{lead}) will have the same effect as the via inductance. This inductance can be minimized in the design of the transition between the package and the PWB.

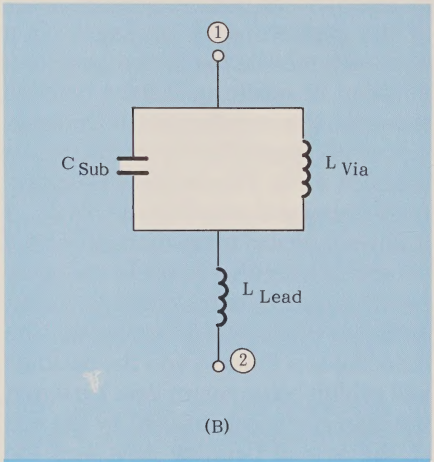


Figure 3B. An electrical model of the metal via, ceramic base and kovar leadframe.

A second way to model the package is to think in terms of distributed effects. In this approach, the added length in the ground current path is modeled as a series stub transmission line terminated with the effective inductance of the vias, as shown in Figure 4. This model assumes that the transmission line connected to the package is a microstrip line as was used in the test fixture. Although the "suck-out" frequency is very sensitive to the value of the inductor and the transmission line impedance, a value of 0.40 nH and 9 ohms, respectively, gives good agreement with the actual data taken for the SMFLAT. The value of the inductor is derived from a formula for a hollow conductive cylinder(s) and the characteristic impedance is formed by the lead frame and the ground plane. This model is satisfying because it predicts the frequency response after the resonance.

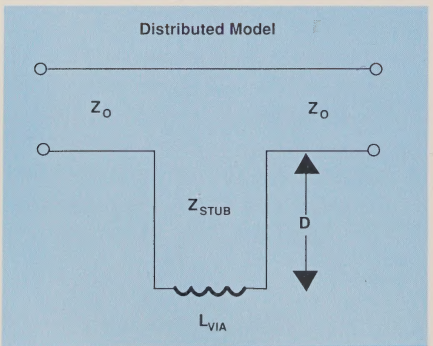
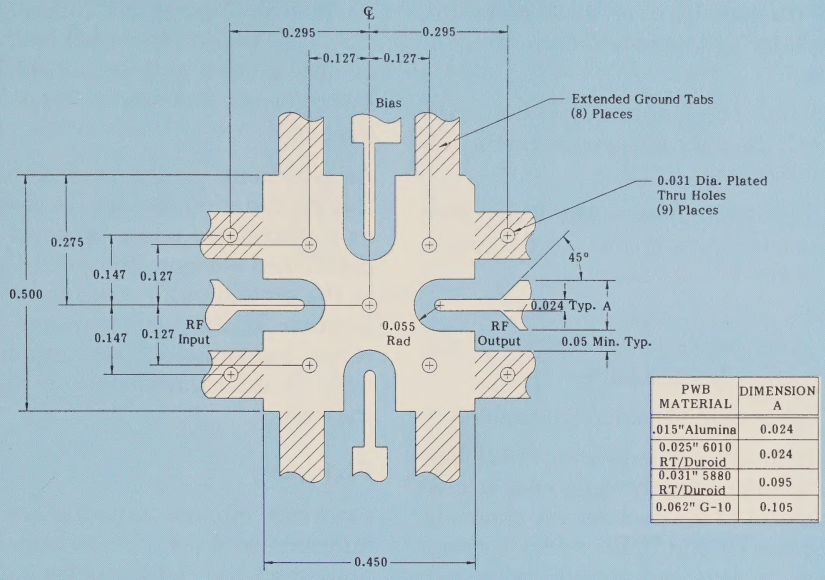


Figure 4. An electrical model of the surface-mount packages using distributed elements. The length, D, is the distance between the center of the lead and the closest ground via.

In summary, the insertion loss of the packages is improved by reducing the shunt capacitance and series inductance, since both of these elements produce a low-pass frequency response and cause a high frequency roll-off. By maintaining a good impedance match among the packages, their mounting surfaces, and the package interconnections, the return loss will be improved.

Grounding

The use of many ground vias inside the package and equally as many plated through-holes connecting the package to the ground of the printed-wiring board insures a good RF ground connection, improved isolation, and reduces the possibility of oscillations in amplifiers. Printed-wiring-board layouts using ground vias located underneath the packages as well as adjacent to the packages have been designed to maximize both electrical and mechanical properties. These layouts are shown in Figure 5A and B, and the electrical performance of the SMTO-8 package mounted to various PWB materials



PWB MATERIAL	DIMENSION A
.015"Alumina	0.024
0.025" 6010 RT/Duroid	0.024
0.031" 5880 RT/Duroid	0.095
0.062" G-10	0.105

Figure 5A. Printed-wiring-board layout for the SMTO-8: 9-hole configuration.

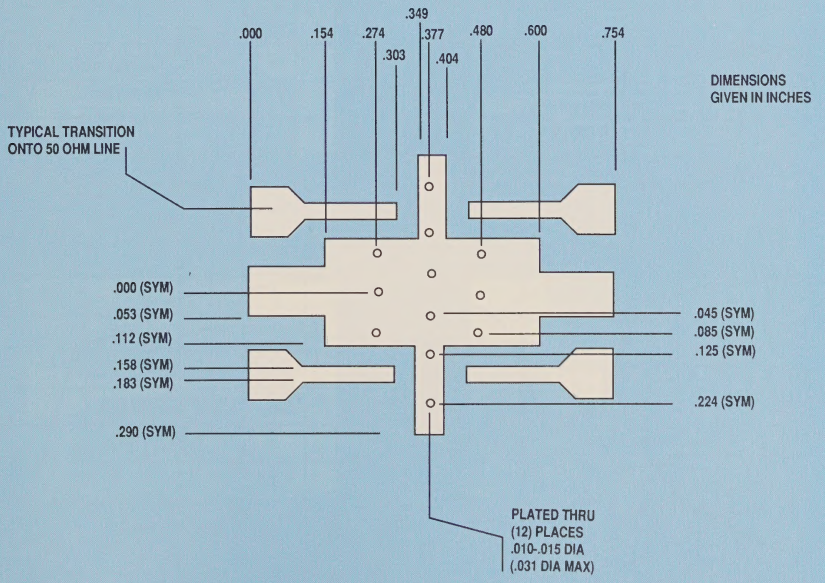


Figure 5B. Printed-wiring-board layout for the SMFLAT: 12-hole configuration.

using this layout is shown in Figures 6A through 6D. For these plots, the package contained a 50-ohm through-line.

The use of plated through-holes underneath the package presents some difficulties with:

1. Reduction in the solder fillet, since solder flows into the plated through-holes during reflow.
2. Rework is more difficult due to thick solder plugs formed in the plated through-holes.
3. Inspection of solder connections.

Alternative printed-wiring-board layouts with plated through-holes located adjacent to the package are shown in Figures 7A and B. Electrical performance is degraded slightly when the ground vias are not located underneath the package, as is shown for the SMTO-8 in Figures 8A through 8D. This degradation is caused by the increased ground inductance which, in turn, lowers the upper cut-off frequency.

As was done for the package itself, this degradation can also be modeled as a distributed effect. Modeled as a distributed element, the extra length in the ground path, presented by the position of the vias, appears as a series transmission line terminated with an inductance equal to that of the vias.

Fixturing

Once the internal capacitances and inductances of the package have been minimized, the problem of testing this new device becomes an issue. As with

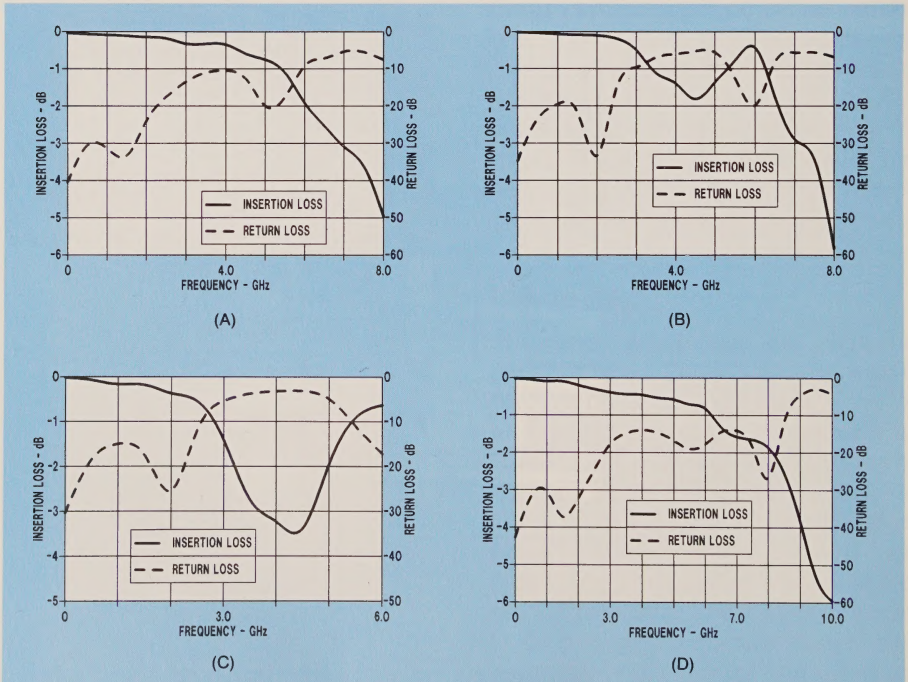
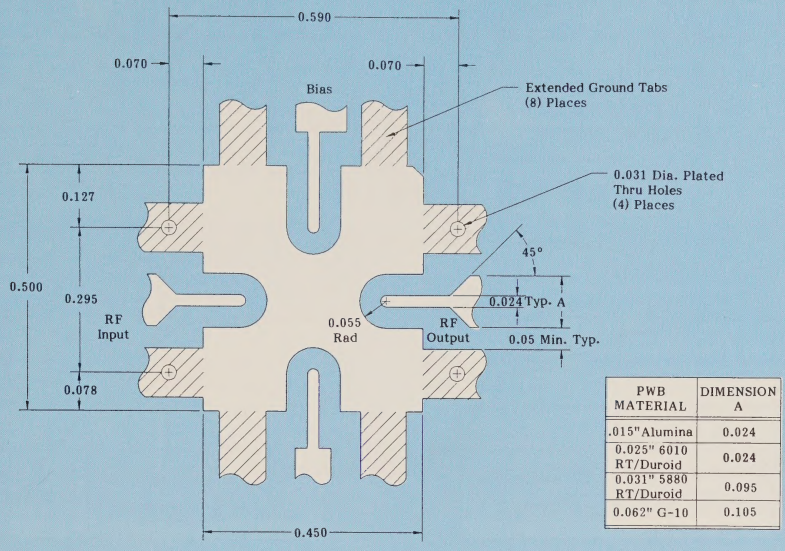


Figure 6. Insertion loss and return loss of the SMTO-8 package mounted with the 9-hole configuration on: A) 0.062" G10, B) 0.025" 6010 RT/Duroid®, C) 0.031" 5880 RT/Duroid® and D) 0.015" 96% alumina.



PWB MATERIAL	DIMENSION A
.015"Alumina	0.024
0.025" 6010 RT/Duroid	0.024
0.031" 5880 RT/Duroid	0.095
0.062" G-10	0.105

Figure 7A. Printed-wiring-board layout for the SMTO-8: 4-hole configuration.

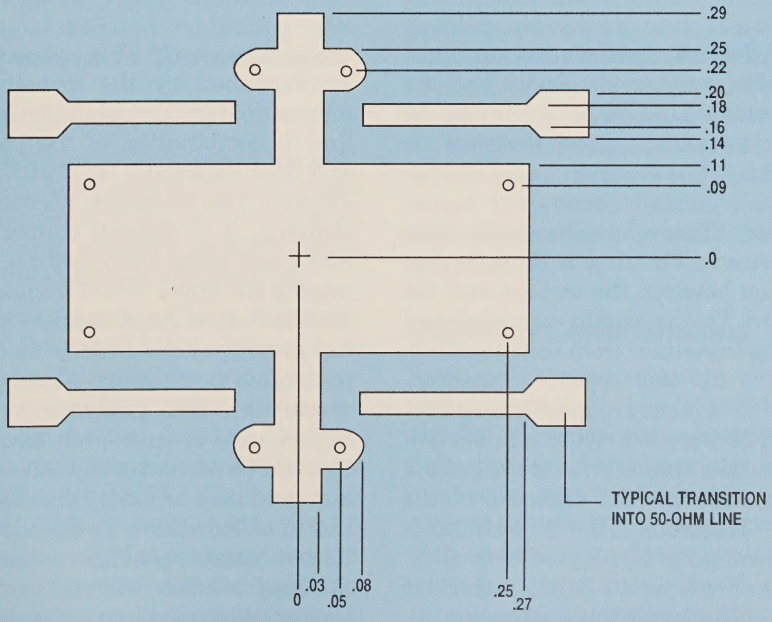


Figure 7B. Printed-wiring-board layout for the SMFLAT: 8-hole configuration.

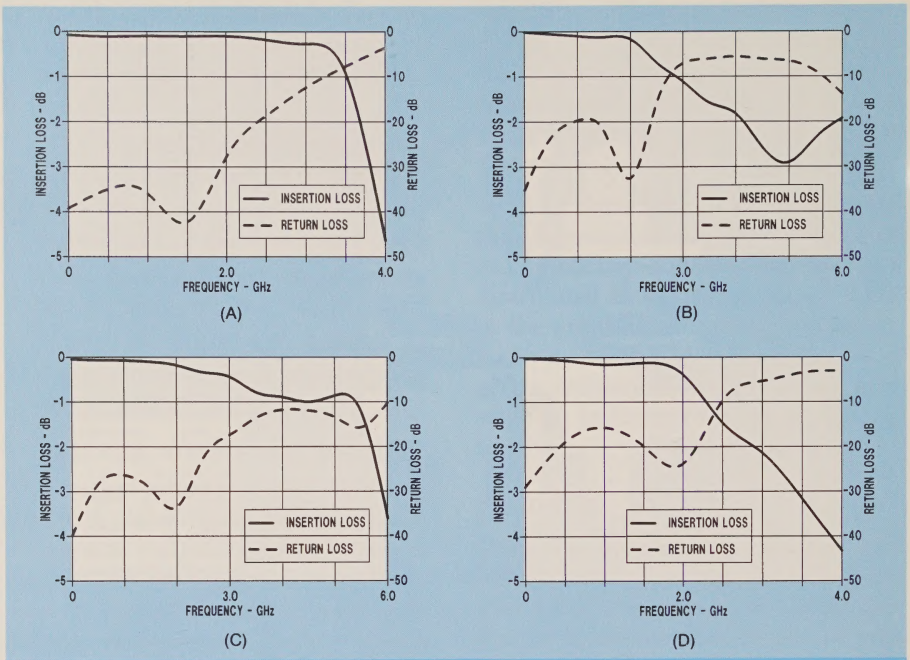


Figure 8. Insertion loss and return loss of the SMTO-8 package mounted with the 4-hole configuration on: A) 0.062" G10, B) 0.025" 6010 RT/Duroid®, C) 0.031" 5880 RT/Duroid®, and D) 0.015" 96% alumina.

most devices, the fixturing and mismatches between the device and the test set-up need to be minimized in order to achieve good electrical response.

The test fixtures have two main areas of concern. The first is the interconnection between the test set and the fixture. This is usually accomplished with a transition from coax to microstrip. With this type of transition, there is a shunt capacitance introduced between the center conductor of the coaxial connector and the ground plane, through the dielectric of the filler substrate. This transition is fairly common and is used to frequencies as high as 40 GHz [2], which is very adequate for this application.

The second and most important interconnection is between the fixture and the package itself. This connection is accomplished by the transition of microstrip (the filler substrate) to stripline (a combination of the package and filler substrate), as illustrated in Figure 9. This transition, microstrip-to-stripline, is a difficult transition to make, and is the main factor in determining the upper cut-off frequency of the test fixture. As shown in Figure 9, the ground plane directly under the package is too close to the lead (center conductor); this produces a shunt capacitance or mismatch loss. This loss can be minimized by introducing a ground step or cavity directly after the filler substrate. In addition, the filler substrate should not extend past the lead as this will produce more ground-plane coupling and loss. This test-fixture design operates up to 7.0 GHz with only 1.0 dB of insertion loss.

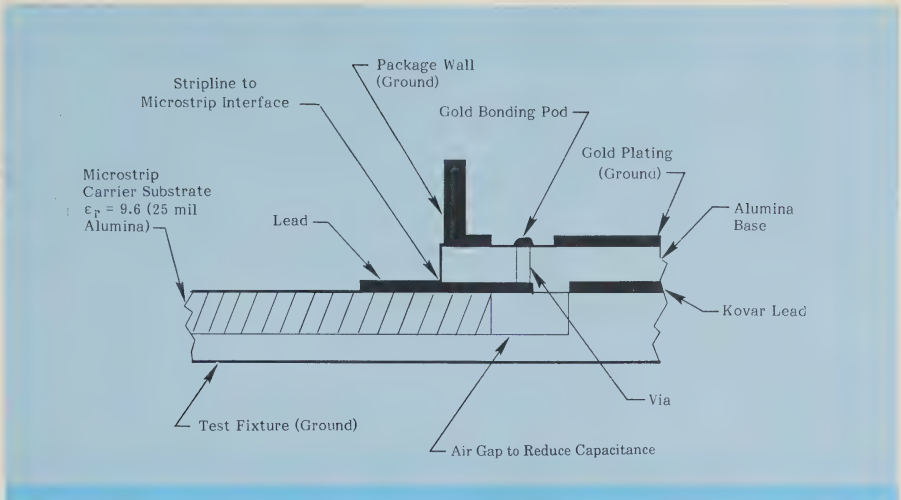


Figure 9. A cross-sectional view of the interface between the test fixture and the surface-mount package.

With the use of open, short, load and through-calibration techniques, the operational goal of 6 GHz has been achieved for the fixture. Further improvement in the performance of the test set may be available through the use of different calibration techniques such as the TRL method [3,4].

Electrical Comparison

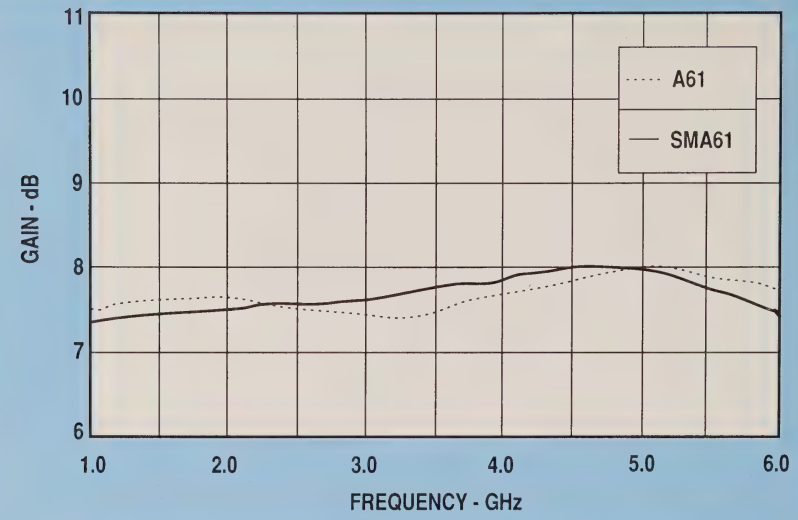
The electrical performance of the new surface-mount products has been tested and compared to the performance of the existing standard products using the same alignment configuration.

The results shown in Figure 10 demonstrate that the TO-8 version and SMTO-8 counterpart are virtually identical, thus making this a drop-in replacement to any existing TO-8 in next-generation surface-mount boards. Similarly, the SMFLAT version displayed slightly better performance compared to its flat-pack counterpart shown in Figure 11. All other products transferred into the surface-mount package achieved performance that was equal to or better than their conventional counterpart.

Consequently, the design and development of these packages has allowed the placement of Watkins-Johnson Company's entire product line of TO-8 (0.5-inch Dia.) and flat-pack amplifiers, mixers, attenuators, limiters, frequency doublers and hybrids, in surface-mount packages with no degradation in performance. Since the TO-8 and the flat-pack versions have been established in the industry for years, the use of these surface-mount packages will drastically reduce the system designer's overall risk when moving to surface-mount technology.

Mounting Considerations

Watkins-Johnson Company's surface-mount products can be mounted on a number of printed-wiring-board materials, including etched-copper board materials and thin/thick-film on ceramic materials. Ceramic materials, such as alumina, closely match the package's thermal expansion coefficient with good electrical performance. However, most systems today are designed using etched copper-backed boards, such as G10/FR4 and Duroid®,



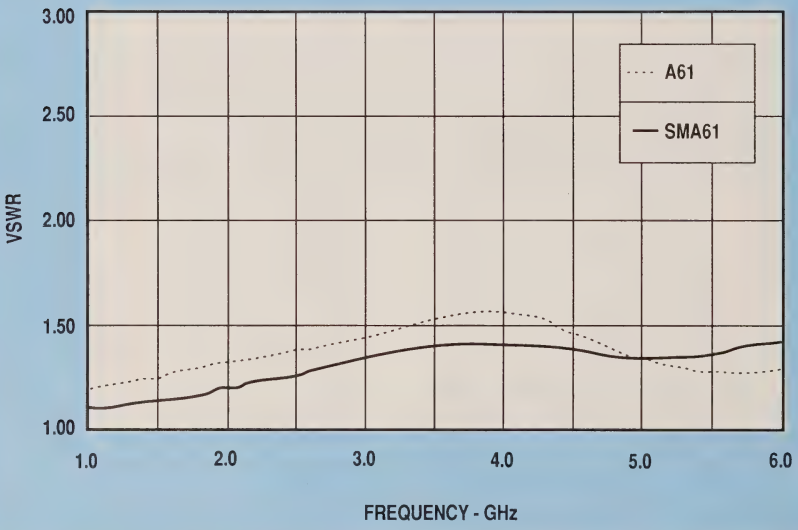


Figure 10. Electrical performance comparison of the A61 amplifier in TO-8 and SMTO-8 packages.

all of which place additional constraints on the system designer in the areas of thermal coefficient of expansion (TCE) mismatches and thermal conductivity of the board material selected. Table 1 compares the significant electrical, mechanical, and thermal properties of various printed-wiring-board materials.

The reliability of any surface-mount attachment is directly dependent on the board type, solder type, and mounting procedure used. Currently, a study is being done at Watkins-Johnson Company to produce guidelines for mounting surface-mount packages for various combinations of variables. This study will provide guidelines for

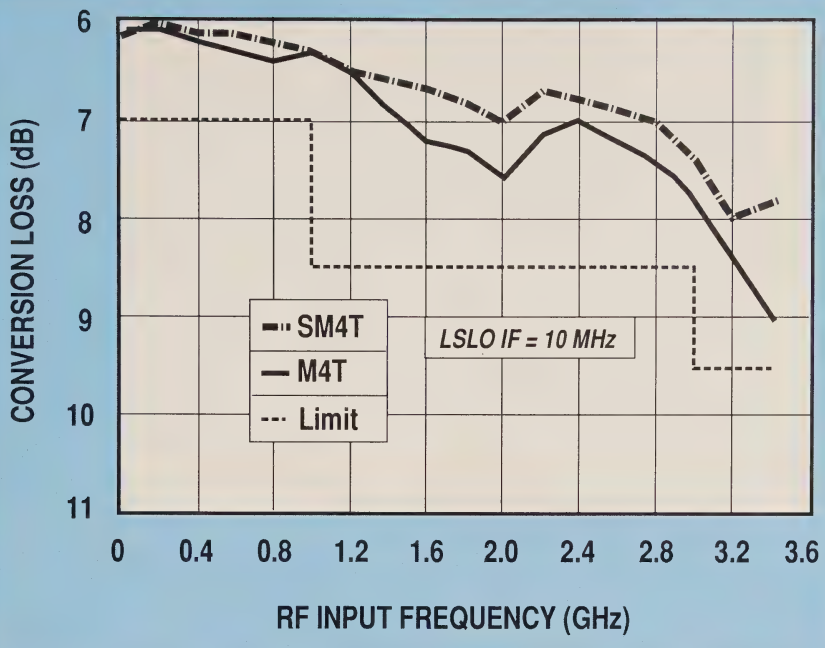


Figure 11. Electrical performance comparison of the M4T mixer in the flat-pack and SMFLAT packages.

Material Properties of Selected Printed-Wiring Boards

Material	Board Thickness (In)	Dielectric Constant	Coefficient of Thermal Expansion (X 10^{-6}/°C)	Thermal Conductivity (W/M/°C)
96% $A1_20_3$	0.015	9.6	6.2	25
RT/Duroid* 6010	0.025	10.5	X = 2.2 Y = 2.2 Z = 1.7	0.41
RT/Duroid* 5880	0.031	2.2	X = 2.2 Y = 3.2 Z = 28.3	0.26
FR4/G-10	0.062	5.2	10–15	0.29

*RT/Duroid is a registered trademark of Rogers Corporation, Microwave Materials Division, Box 3000, Chandler, AZ 85224, (602) 961-1382.

Table 1. Electrical and mechanical PWB properties.

some of the more common materials and processes available.

The printed-wiring-board layout is designed such that the package aligns itself due to surface-tension effects during solder reflow. The layout has the same width as the package width to maintain proper alignment in the x-direction. The y-dimension on the layout is made larger to allow for an inspectable solder fillet. The lead pads serve to align the device in the y-direction. Figures 5 and 7 show the layout for a typical printed-wiring-board material.

A preliminary study was done on G10 PWB's, which is one of the more common board materials. G10 also presents a significant mechanical test for mounting procedures, since its thermal expansion is 3 times that of the package.

The solder selected was Sn63 (63% Sn, 37% Pb), which is clearly the industry standard for a number of reasons. Sn63 solder has a melting point of 183-degrees centigrade, which is high enough to exceed the 150-degree centigrade operating temperature of most systems, and is low enough that internal component materials are not damaged during reflow. It has been found to be the most solderable of the Sn/Pb compositions and is very ductile (reaching 75% elongation at room temperature), a property that is extremely desirable in the surface-mount attachment, which may have to endure a good deal of stress over temperature [5,6]. The one draw back of Sn63 solder in this application is a phenomena called "scavenging." This occurs when gold plating from the package migrates into the solder joint during reflow, which may cause embrittlement of the solder joint. As a result, careful selection of the metalization scheme must be made to prevent scavenging. Pretining the package/leads with Sn63 solder paste with RMA flux reduces the gold concentration and produces a stronger joint. Alternatively, Indium alloy solder pastes, which have a low tendency to dissolve gold, may be used.

Solder paste thickness is also expected to effect the quality of the joint directly. For the pad geometry shown in Figures 5 and 7, the minimum workable thickness is approximately 0.006-inch, which is roughly the point at which an acceptable concave fillet forms. The maximum thickness is approximately 0.012-inch, the point at which the fillet becomes convex or "bulbous."

An experiment was conducted to determine the optimum SN63/Pb37 solder thickness; both SMTO-8 and SMFLAT packages were mounted to G10 printed-wiring boards using various layouts and solder thicknesses. The completed assemblies were then subjected to thermal cycling (-50°C to +125°C per MIL-STD-883C, method 1010.6) during which contact resistance and visual inspection was performed periodically. The results of this experiment are shown in Table 2. The optimum thickness of Sn63 was found to be 0.007-inch to 0.010-inch. Silk-screening techniques can control paste thickness well enough to keep it in the optimum ranges, the thickness being a function of the screen mesh, emulsion thickness, and printer set-up parameters.

The solder reflow was performed in a Watkins-Johnson convection/IR furnace. A typical temperature profile is shown in Figure 12. The profile reflects the three distinct heating stages (preheat, reflow and cooling) recommended in automated reflow processes to ensure reliable finished joints. These temperatures were taken in the ambient air immediately surrounding

Package Type	PWB Layout	PWB Material	Wet Solder Thickness (In)	No. of Cycles Passed*
SMTO-8	Fig #5A	G10 (.062″ thick)	.004	500
SMTO-8	Fig #5A	G10 (.062″ thick)	.006	1000
SMTO-8	Fig #5A	G10 (.062″ thick)	.009	700
SMTO-8	Fig #7A	G10 (.062″ thick)	.004	1000
SMTO-8	Fig #7A	G10 (.062″ thick)	.006	1000
SMTO-8	Fig #7A	G10 (.062″ thick)	.009	1000
SMFlat	Fig #7B	G10 (.062″ thick)	.004	300
SMFlat	Fig #7B	G10 (.062″ thick)	.006	300
SMFlat	Fig #7B	G10 (.062″ thick)	.009	300

*Thermal cycling per MIL-STD-883, method 1010.6 (–50°C to +125°C)

Table 2. Summary of temperature cycling SMTO-8 and SMFLAT assemblies mounted on .062″ thick G10 boards using various thickness of SN63 solder paste.

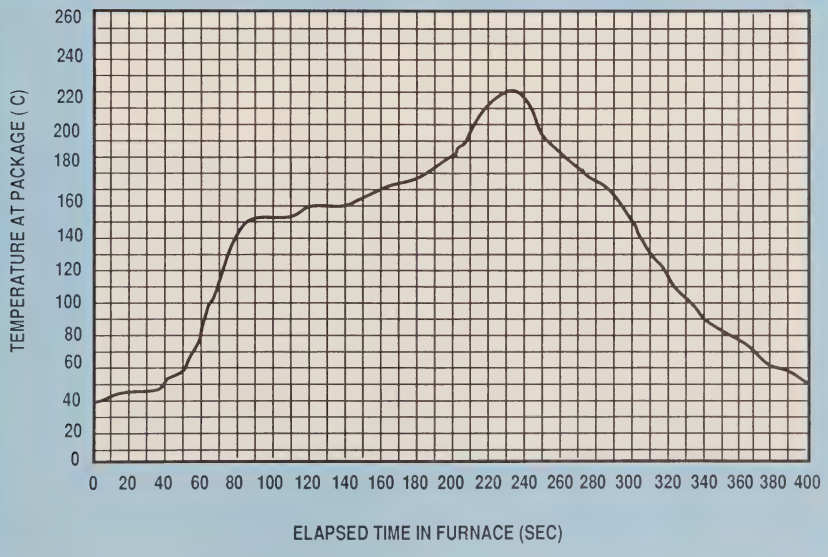


Figure 12. The temperature profile used to reflow the solder during package mounting.

the part (<1-inch away). It is recommended that the temperature be limited in the reflow stage to a maximum of 230°C. Temperatures greater than 200°C may be sustained for up to 1 minute, and temperatures greater than 220°C for up to 30 seconds. Watkins-Johnson Company has conducted studies to verify that these intermittent high temperatures will not internally damage the components. The studies included both mechanical and electrical evaluations before and after the parts were subjected to these temperatures.

Reliability and Screening

Watkins-Johnson Company's line of surface-mount products is designed and manufactured to meet the stringent performance and quality requirements of MIL-STD-883, Method 5008. The packages are capable of meeting the requirements of MIL-STD-883, Method 5008.1 packaging requirements per Table 3.

Thin-film hybrid surface-mount products are designed and manufactured with the same materials and assembly techniques already proven in the TO-8 product line. This similarity in design and construction allows the system designer the same level of confidence in system integrity.

All Watkins-Johnson surface-mount amplifier products are offered with a standardized environmental screening option designated "S" series. The "S" series provides a cost and time-effective approach to meeting the requirements commonly found on many airborne, ground-mobile, shipboard, and missile applications. The screening is per MIL-STD-883, Method 5008, as outlined in the Watkins-Johnson RF and Microwave Component Designers' Handbook.

Conclusion

In choosing or designing surface-mount packages, special attention was placed on RF performance, size, structural integrity for mounting, inspectable solder connections, and hermeticity. Direct compatibility with existing TO-8 and flat-pack models eases the transition to their surface-mount counterparts and allows system designers the freedom to choose from a wide variety of RF components.

Package Testing Performed Successfully on SMTO-8 Packages

Test (MIL-STD-883)	Method	Condition
Thermal Shock	1011	C, -65° to +150°C
High Temperature Bake	1008	F, 300°C
Solderability	2003	
Hermeticity	1014	A_4
Salt Atmosphere	1009	A, 24 Hours
Lead Integrity	2004	A, B_4

Table 3. Environmental package screening.

References:

1. Dexter, Charles E. "Design Considerations for Miniaturized Receivers," *Watkins-Johnson Company Tech-notes*, Volume 16, No. 5 September/October 1989.
2. Wiltron, K-Commentary, No. 2, November 1986.
3. "Network Analysis: Applying the HP8510 TRL Calibration for Non-Coaxial Measurements," *Hewlett-Packard Product Note 8510-8*, October 1987
4. Engen, G. F. and C.A. Hoer. "Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-port Automatic Network Analyzer," *IEEE Trans. Microwave Theory and Techniques*, December 1979.
5. Evans, John W. "An Overview of Thermally Induced Low Cycle Fatigue in Surface Mounted Solder Joints," *Surface Mount Technology,* February 1989.
6. Fincham, Eric "Finish with Solderability," *Circuits Manufacturing,* February 1988.
7. Seieroe, Louis M., Kenneth S. Ledford, Timothy J. Blaney and Louis Hsiao, Watkins-Johnson Company, "Surface-Mount Products Match TO-8 Performance and Availability," *RF Design* Magazine, October 1989.

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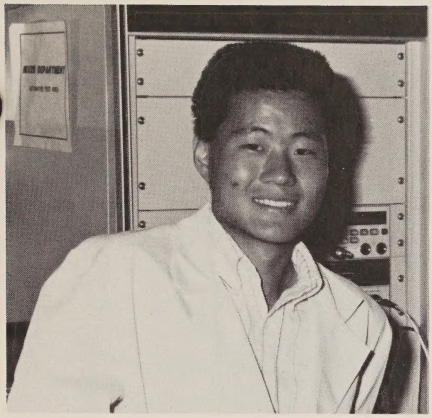

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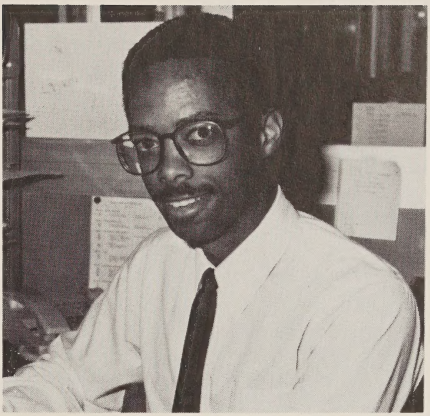

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