GBPPR 'Zine

"I also believe that a lot of gun owners would agree that AK−47s belong in the hands of soldiers, not in the hands of criminals...   That they belong on the battlefield of war, not on the streets of our cities."

−−− Quote from Barack Hussein Obama (a.k.a. Barry Soetoro), a Kenyan−born Marxist Muslim usurper and puppet for globalist bankers. Oh, Barry, the U.S. military doesn't use AK−47s...

"Every citizen should be a soldier. This was the case with the Greeks and Romans, and must be that of every free state."

−−− Quote from Thomas Jefferson, third President of the United States.

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1. GENERAL

1.01   This section describes the peripheral unit controller (PUC) when used with the No. 1 or the No. 1A Electronic Switching Systems (ESS). The PUC (J1A098B-1) is a universal microprocessor controller which provides control of certain frames of equipment. For example, the PUC controls the digital carrier trunk (DCT) frame and data link information for the Remote Switching System (RSS), electronic tandem switching (ETS), and common channel interoffice signaling (CCIS).

1.02   This section is reissued for the reasons listed below. Revision arrows are used to emphasize the more significant changes. Equipment Test Lists are not affected.

(1) Add information related to the scanner answer memory

(2) Add information for internal buses

(3) Add information related to the power bus and control

(4) Add information related to the peripheral unit parity feature

(5) Add information related to the digroup buffer circuit.

1.03   Abbreviations used in this section are listed in Part 8.

1.04   The PUC mounts in a standard universal trunk frame and is 24 inches high. It is a self-contained, pluggable unit, equipped with its own power supplies, control panel, and fusing. The PUC is used in a one bay frame for the data link (DL) application and a three-bay frame for the DCT application (Fig. 1).

2. PERIPHERAL UNIT CONTROLLER

2.01   Orders and signaling information are sent to the PUC via the peripheral unit address bus (PUAB) and central pulse distributor (CPD) (Fig. 2). The communication loop is completed with the response messages returned to the ESS on the scanner answer bus (SCAB). The peripheral bus circuit contains the bus receivers and drivers. Operational orders and maintenance orders are sent to the PUC, and either by command or timing are acted upon with a reply message returned via the SCAB. The reply messages contain operations completed, maintenance data, error alarms, and audit reports.

2.02   ▶Each PUC frame in an ESS office requires 44 unipolar and 12 bipolar CPD points plus 24 scan points of which 20 are direct and 4 superviosry.◀

MICROPROCESSOR CONTROLLER

2.03   A PUC frame consists of two identical microprocessor based controllers. In normal operation both controllers run in a matched mode (DUPLEX) executing identical instruction streams. Controllers are synchronized by means of a shared clock. Each controller receives orders from the ESS and executes the commands. The processing is performed and outputs are matched, but only the controller designated as active outputs to the system. In case of a failure the other controller would be configured to be the output device. The controller hardware is mounted on plug-in circuit packs which insert into two shelves with the power bus and converters as a part of the PUC. The bus interface units are mounted in a third shelf at the top of the PUC.

2.04   Each PUC controller (Fig. 3) consists of four functional areas—the ESS/PUC interface, hardcore, memory, and the PUC/peripheral interface.

A. Interface

2.05   The ESS/PUC interface consists of a mode and enable (MEN) circuit, a first in-first out (FIFO) buffer, and a scanner answer memory (SCAM).

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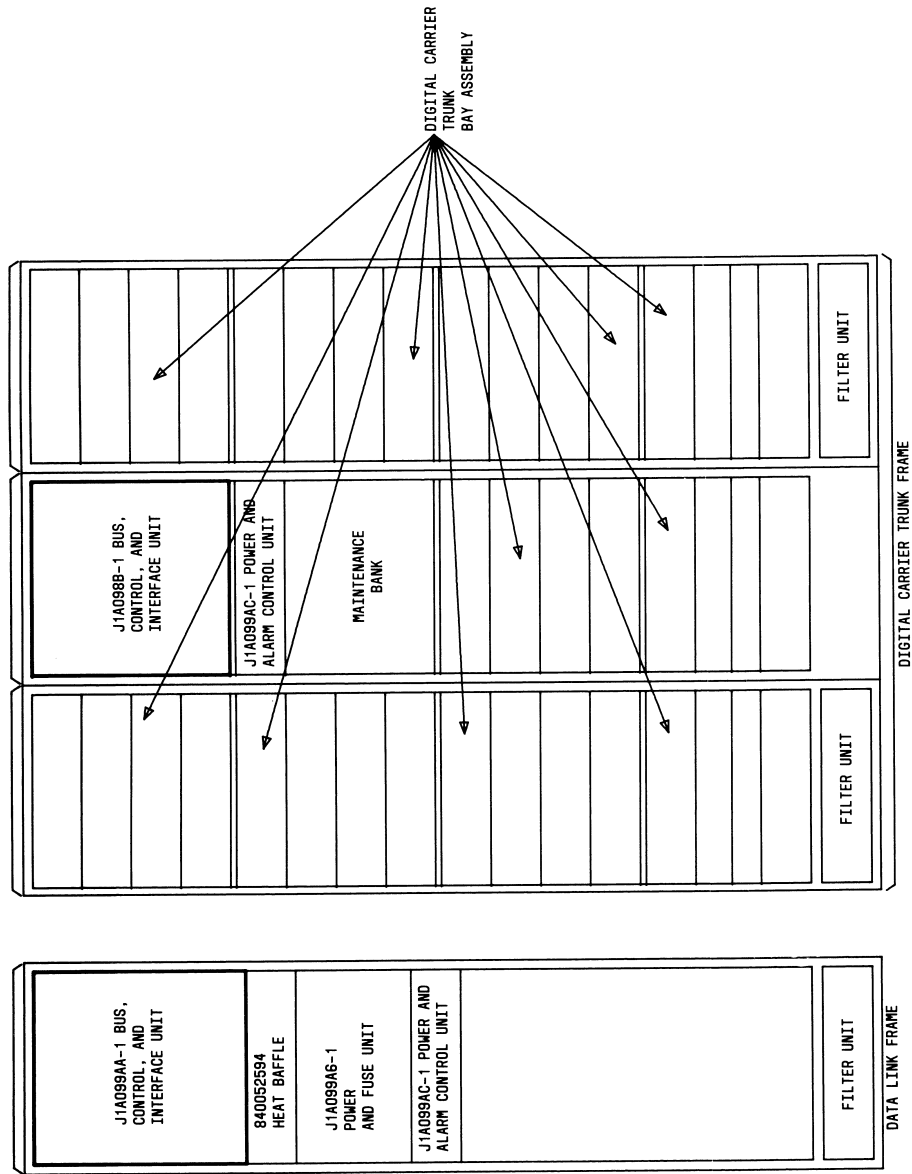
Fig. 1—Peripheral Unit Controller/ Data Link and Digital Carrier Trunk Frames

SCANNER ANSWER
BUS 0
PERIPHERAL UNIT
ANSWER BUS 0
CENTRAL
PULSE
DISTRIBUTOR
(EVEN)

SCANNER ANSWER
BUS 1
PERIPHERAL UNIT
ANSWER BUS 1
CENTRAL
PULSE
DISTRIBUTOR
(ODD)

PERIPHERAL BUS CIRCUITS

FROM
CENTRAL
PULSE
DISTRIBUTOR
TO SCANNER

FROM
CENTRAL
PULSE
DISTRIBUTOR
TO SCANNER

CONTROLLER 0
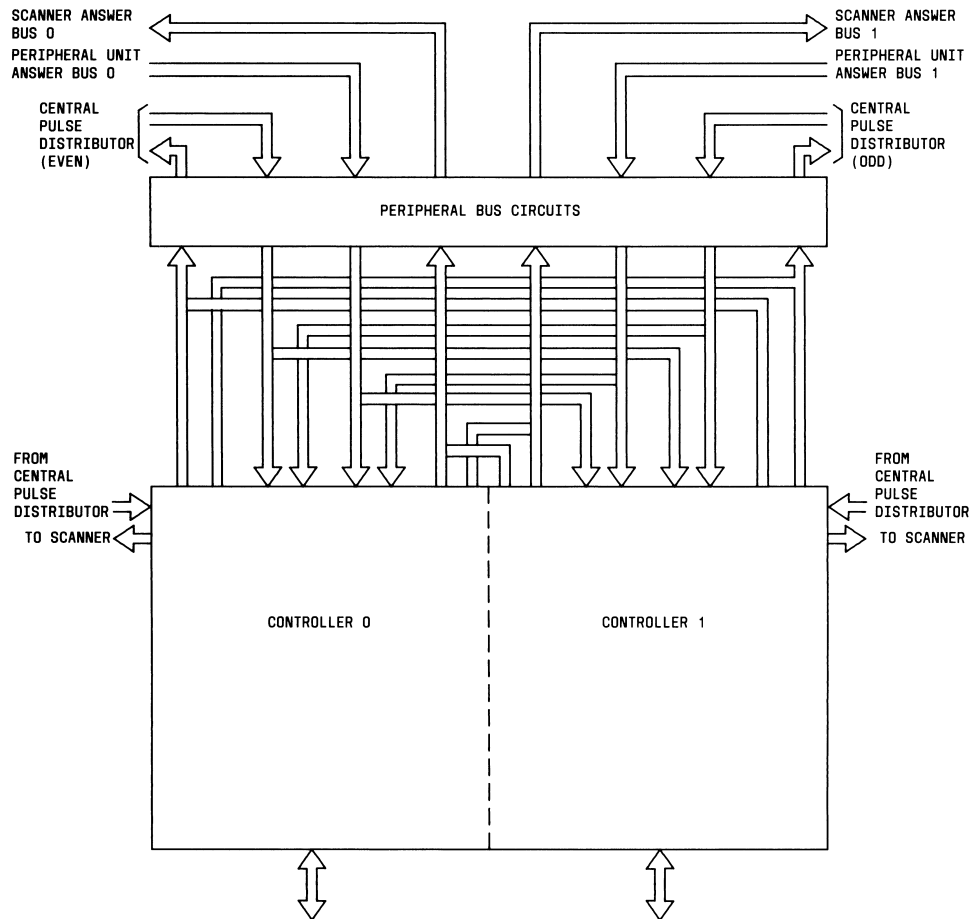
CONTROLLER 1

Fig. 2—Interface Bus Circuit

SECTION 231-037-020
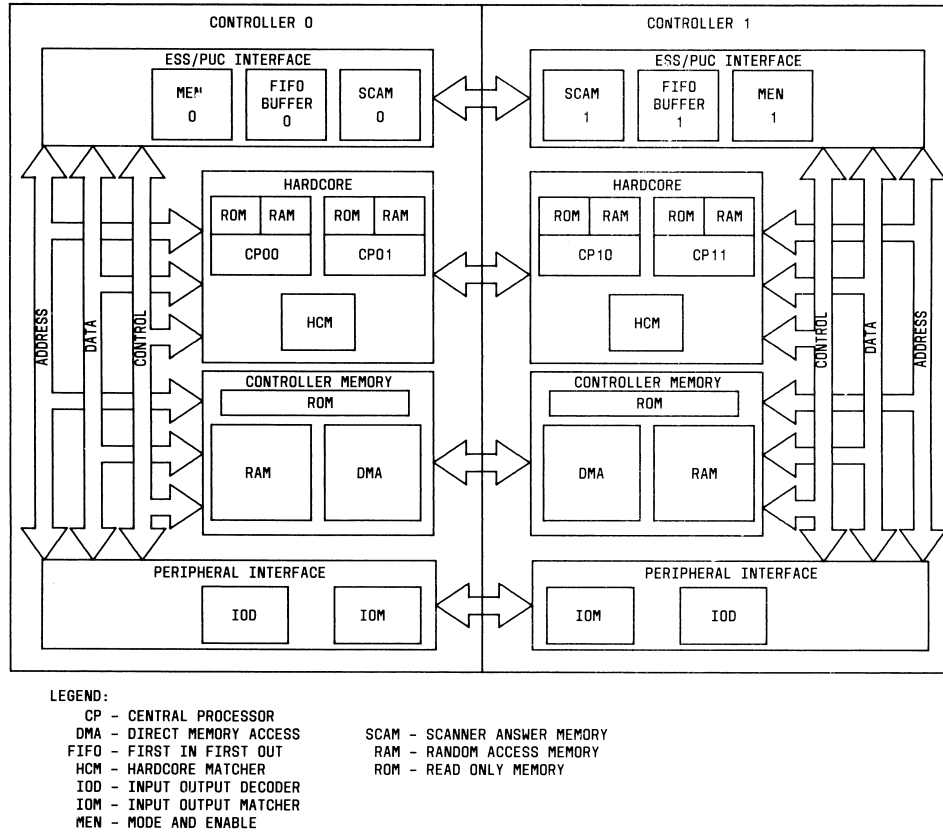
Fig. 3—Peripheral Unit Controller Block Diagram

LEGEND:
CP – CENTRAL PROCESSOR
DMA – DIRECT MEMORY ACCESS   SCAM – SCANNER ANSWER MEMORY
FIFO – FIRST IN FIRST OUT   RAM – RANDOM ACCESS MEMORY
HCM – HARDCORE MATCHER   ROM – READ ONLY MEMORY
IOD – INPUT OUTPUT DECODER
IOM – INPUT OUTPUT MATCHER
MEN – MODE AND ENABLE

2.06 ◆The MEN circuit allows the ESS to monitor and control the maintenance states of the controller, enable the FIFO buffer, and monitor the controller for failures. It also controls the out-of-service lamps on the power and alarm control unit.◆

2.07 The MEN circuit contains a set of mode flip-flops which allows the ESS to control and monitor the maintenance states of the associated PUC controller. These flip-flops are called master, lockout, scanner answer bus access, and divorce. Master flip-flops are duplicated and matched for reliability. When both master flip-flops are set, the associated controller has access to the peripheral units. In addition to ESS control, the PUC hardcore may also change the state of the master flip-flops. When the lockout flip-flop is set, the hardcore is prevented from changing the master flip-flops. When the scanner answer bus access flip-flop is set, the PUC controller has access to the scanner answer bus thus allowing the associated SCAM to return data to the ESS. When the divorce flip-flop is set, the enable inputs to the FIFO buffer are inhibited and no ESS orders are input to the FIFO buffer.

2.08 The FIFO buffer enable circuit receives enables from the ESS and produces the necessary signals to load the FIFO buffer from the PUAB.

2.09 The MEN circuit contains four failure flip-flops controlled by the hardcore plus scanner drivers which allow the ESS to monitor the state of the failure flip-flops. These flip-flops may be reset by the ESS or PUC. Internal fault flip-flops are set when any fault in the controller processor is detected by hardware. There is one internal fault flip-flop for each of the two controller processors contained in the hardware. The SCAM failure flip-flop is set when the hardware detects any fault in the SCAM. The hardcore failure flip-flop is set when a mismatch between hardcores is detected.

2.10 The FIFO buffer, also called the data input FIFO buffer (DIF), consists of a memory with the control circuitry required to make it a first in-first out queue. ESS orders are input to the FIFO buffer from the PUAB. The FIFO buffer is controlled by the ESS via the MEN circuit. The ESS orders are unloaded periodically by the hardcore. The hardcore controls the FIFO buffer using the DIF controller (DIFC) circuit. The ESS sends a 24-bit word to be loaded but the PUC hardcore unloads them in 8-bit words.

2.11 ◆Sixteen-bit reply and maintenance messages are sent from the hardcore to the SCAM. The SCAM consists of random access memory (RAM) which temporarily stores data. The ESS sends enable signals and addresses to return data via the SCAB. The SCAM controller (SCAMC) controls the loading and unloading of the SCAM.

2.12 The SCAM circuitry returns a 16-bit data word, an all seems well (ASW) bit, a parity bit, and a check bit back to the ESS over the SCAB. The ASW bit is used to indicate that the scanner circuit has functioned properly and that the information being sent to the ESS CC is correct. The parity and the check bit are returned for the PUP feature (paragraph 4.06).◆

B. Hardcore

2.13 The controller hardcore consists of two central processors (CPs) and associated memory. A hardcore matcher is also included.

2.14 The central processor is a BELLMAC*-8 microprocessor. This microprocessor runs on a program contained in its read only memory (ROM).

2.15 The hardcore memory consists of RAM and ROM for each individual central processor. The RAM stores transient data for the processor. The ROM is in the form of erasable programmable read only memory (EPROM). This memory stores the program for the processor and can only be read. The EPROM is used so that the circuit pack can be reused if a program change is made (see paragraph 4.09).

2.16 The hardcore matcher (HCM) compares the two central processor outputs for fault detection.

C. Controller Memory

2.17 The controller memory consists of RAM, a direct memory access (DMA), and ROM. The RAM is used to store transient data associated with the controller. The DMA is used to update the RAM of a controller which is being brought back in service. The DMA copies the RAM contents of the active controller into the RAM of the controller being initialized. The ROM is in the form of EPROM and is programmed with application firmware.

*Trademark

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D. ◆Internal Buses

2.18 The internal PUC bus system consists of an address bus, data bus, and control bus. The address bus is used to communicate the address of memory locations for read and write operations. The data bus consists of eight data bits and one even parity bit. The bus is bidirectional and the direction of data transfer is determined by the system's read and write control signals. The control bus communicates control signals and fault indications.◆

E. Peripheral Interface

2.19 The PUC/peripheral interface consists of an input-output decoder (IOD) and an input-output matcher (IOM).

2.20 The IOD decodes commands from the PUC to be used by the peripheral circuits. It also sends enables to the line interface units used for DL applications. The IOM compares certain outputs of the controllers before being sent out to the peripheral units.

POWER BUS AND CONTROL

2.21 The power is provided to converter packs located on the right side of the shelf for DCT and below the PUC for the DL application. Distribution of +5 and +12 volts to the circuit packs is handled by the converters and regulators (Fig. 4). Power indicators and manual switches are provided on the control panel (Fig. 5). Test jacks are provided to measure power levels at the panel. The PUC controllers (called controller 0 and 1) are supplied by a separate power bus for reliability. This arrangement allows one controller to be removed for maintenance with no interruption of power to the other controller.

2.22 ◆Only one of the two PUC controllers or data buses can be taken out of service at any time. This is accomplished by the system and can be requested manually by maintenance personnel or automatically requested due to faults detected by the system. The manual request is made via the teletype or by operating the REQ INH key on the PUC power alarm control unit (Fig. 5). The out-of-service lamp will light when the system takes the controller out of service for any reason. The actual removal of power can only be done manually at the PUC power and alarm control unit by operating the appropriate OFF key for either the controller or data bus circuit. The

power removal and restoral procedure is contained in Section 231-105-302.◆

3. OPERATION

3.01 The PUC is a general purpose, microprocessor based controller. The operation of the PUC is different for the different applications depending on the application firmware. However, there are some operations which remain the same for different applications such as the maintenance operations for the microprocessors. For all applications, the PUC operates autonomously using its own timing clock. The PUC receives information from the ESS but acts on the information at the appropriate time in the PUC's program cycle. Returning data from the PUC is accomplished by normal scan orders.

4. MAINTENANCE CAPABILITIES

4.01 The maintenance functions of the PUC may be classified as follows:

- Fault detection and location

- Reconfiguration and recovery.

4.02 Fault detection and location is achieved through hardware fault detection circuits (matching circuits, parity checks, etc), and by frequent self-diagnostic tests.

4.03 The PUC has two controllers —one active and one standby—that normally run in a duplex mode fully synchronized and continuously matched to each other. Each controller contains two microprocessors. Each controller is self-checking, using its own internal diagnostic routines, and the microprocessor's outputs are simultaneously matched to detect faults in the instruction sequence. Faults not detected internally by the microprocessors will be recognized (within microseconds) by the mismatch. This mismatch triggers a diagnostic. Matching is performed on two levels: between the two PUC controller outputs and internally in the hardcore modules. There are also automatically run background diagnostics built into the firmware. Most of the maintenance firmware resides in the HC ROM. Some maintenance firmware is in the controller ROM.

4.04 Reconfiguration of controllers is automatically done if the active controller is determined faulty. The reconfigured operation would put

CONTROLLER O	CONTROLLER 1
55 – 80W @ + 5V ± 5% 1W @ + 12V ± 9%	55 – 80 W @ + 5V ± 5% 1W @ + 12V ± 9%

+5V   +12V   +5V   +12V

| 131 F1
OR 132 AB
DC – DC
CONVERTER | SERIES REGULATOR | 131 F1
OR 132 AB
DC – DC
CONVERTER | SERIES REGULATOR |

−48V   +24V   −48V   +24V
 A   A   B   B

LEGEND:
DC – DIRECT CURRENT
 V – VOLT
 W – WATT
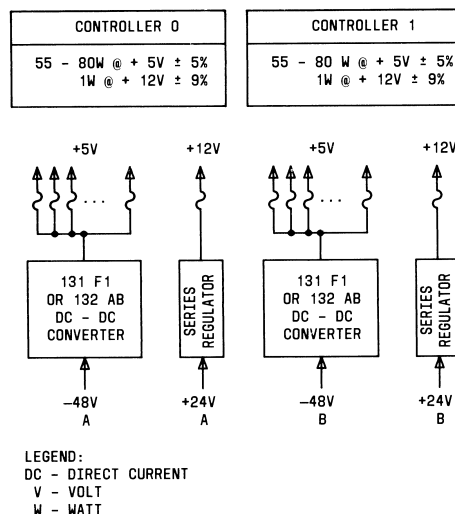
Fig. 4—Power Distribution

the other controller in the active state. If both controllers are diagnosed to have faults, the active controller will continue to output data and signaling for system operation while the out-of-service controller runs diagnostics. The ESS monitors the PUC diagnostics and may request certain diagnostics. The ESS also has ultimate CPD control and can reconfigure the PUC contrary to the PUC controllers. Teletypewriter (TTY) messages indicating PUC faults are output at the time of occurrence via PUC error messages. These faults may be transient in nature causing no reconfiguration or may be hard faults which cause the PUC to reconfigure as part of a recovery action. Controller states are automatically changed by the system to the preferred state; however, they may be changed by maintenance personnel using TTY input messages (IM1A001 or IM6A001). See Table A for the valid PUC states.

4.05 ◆The PUC diagnostic is a special purpose program designed to test the PUC and aid maintenance personnel in locating any hardware faults that might be present. The maintenance procedures for the PUC/DCT are contained in task oriented

practice (TOP) 231-050-015. The maintenance procedures for the PUC/DL are contained in TOP 231-050-027. PK-1A473 is a tutorial and reference manual on how to use the PUC diagnostics in a No. 1 ESS.◆

PERIPHERAL UNIT PARITY

4.06 Peripheral unit parity (PUP) is a maintenance feature which provides parity checking on the SCAB associated with the PUC. The PUP feature requires two additional bits on the duplicated SCAB. One bit is a parity bit which is pulsed whenever the parity over the 16 data bits is even. The other bit is a parity check request bit which is pulsed whenever the PUC identifies itself as a circuit. Pulsing the parity check request bit causes the central control (CC) and signal processor (SP) to check the parity of the 16 data bits and the parity check bit. If the parity check indicates an error, a maintenance interrupt will occur to call in the recovery programs to resolve the problem. Also, an associated interrupt printout message informs the maintenance personnel of the trouble condition that occurred. The CCs and SPs compute the parity of the SCAB without the parity

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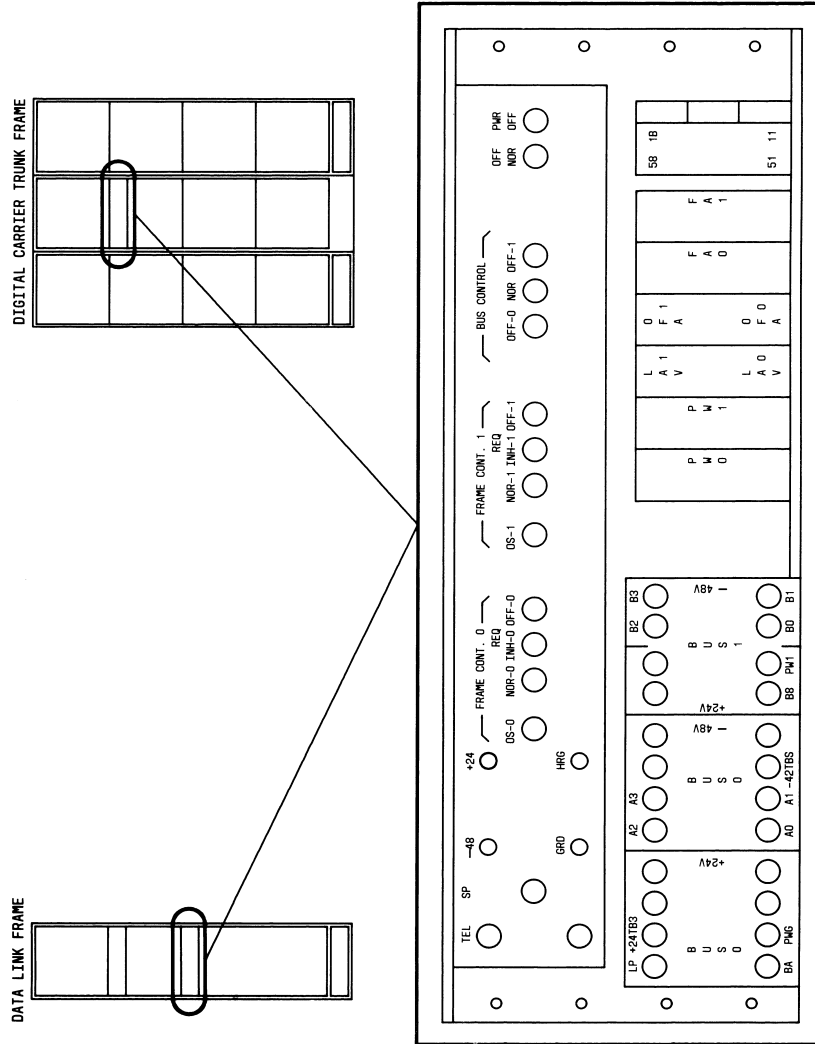
Fig. 5—Power and Alarm Control Unit

TABLE A

VALID PERIPHERAL UNIT CONTROLLER OVERALL STATES

STATE NAME (NOTE)	DESCRIPTION OF STATE
ACTIVE:STBY-SUPPORT	The PUC is running matched between controllers. Both controllers receive all orders from ESS but only the defined ACTIVE controller sends orders to shared periphery.
ACTIVE:OS-OFF-LINE	The controller designated ACTIVE performs the operational function of the PUC while the OS-OFF-LINE controller is being used by maintenance programs for testing (diagnostics). The OS-OFF-LINE controller will be automatically returned to service if a fault occurs on the active controller.
ACTIVE:OS-MANUAL	The controller designated ACTIVE performs the operational functions of the PUC while the OS-MANUAL controller is available for maintenance and test programs. The OS-MANUAL controller will be returned to service if a fault occurs (ERR-ANALYSIS) in the ACTIVE controller.
ACTIVE:OS-FAULT	The controller designated ACTIVE performs the operational functions of the PUC while the OS-FAULT controller has been diagnosed to have a fault. The OS-FAULT controller will be returned to service (ACT-MR) if the ACTIVE controller fails.
ACTIVE:OS-RMVD	The ACTIVE controller performs the operational functions of the PUC while the OS-RMVD controller, having a possible fault, is being diagnosed. Upon completion of diagnostics the OS-RMVD controller moves to the appropriate permanent state.
ACTIVE:UNAV-FORCED	While the ACTIVE controller is operational, the UNAV-FORCED controller has, by maintenance personnel action, been removed from automatic system use. The UNAV-FORCED controller is left in a maintenance access mode.
ACT-MR:OS-FAULT	Both controllers are known to be faulty. The ACT-MR is used for operation with all fault detection turned off. The OS-FAULT controller, also known to have a fault, is locked out.
ACT-MR:OS-RMVD	Both controllers have failed. The ACT-MR controller is known to be faulty, but is used for operation with all fault detection turned off. The OS-RMVD controller, also having failed, is awaiting execution and completion of the diagnostic to move to a permanent state.
ACT-MR:UNAV-FORCED	The ACTIVE controller has failed while the support controller (UNAV-FORCED) is unavailable to the system. All maintenance is removed from the active controller (ACT-MR). The UNAV-FORCED controller was removed from system use by maintenance personnel action and will remain so until future maintenance personnel action is taken.
ACTIVE:OS-PWR-OFF	The ACTIVE controller performs the operational functions of the PUC. The OS-PWR-OFF controller has power removed.
PWR-OFF:PWR-OFF	Both controllers have power removed.

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TABLE A (Contd)

VALID PERIPHERAL UNIT CONTROLLER OVERALL STATES

STATE NAME (NOTE)	DESCRIPTION OF STATE
ACT-MR: OS-PWR-OFF	The designated ACT-MR has a fault but attempts to perform the operatinal function of the PUC. The second controller has power off.
ACTIVE: OS-PWR-OFF	(Last state return). The OS-PWR-OFF controller has power off. After power is restored, it will return to the OS state it was in prior to power removal.
ACT-MR: OS-PWR-OFF	(Last state return). The ACT-MR controller attempts to perform the operational function for the PUC. The second controller has power off but will return to the OS state in which it resided prior to power removal.

Note: The first state name is defining one controller and the second state name (after the colon) is defining the second controller.

check bit and match the results. This parity match provides more immediate detection of certain classes of PUC troubles before they result in C-level interrupts. In addition to the 16 data bits and the 2 PUP bits there is an all seems well (ASW) bit on the SCAB.

4.07 ◆The hardware modifications required to install the PUP feature in a No. 1 ESS office consists of a central control circuit SD-1A105 and a communication bus circuit SD-1A119. The central control circuit equips the CC for communications with the peripheral units. The communication bus circuit provides for maintenance of the peripheral unit bus and improves maintenance of the peripheral addressing system. Additional hardware changes required when the PUP feature is used in an SP office consists of a signal processor circuit SD-1A131. This circuit allows the signal processor to serve as a buffer between the CC and the input/output equipment.

4.08 When the PUP feature is used with the No. 1A ESS, wiring changes are required on the SD-5A010-01/02 central control circuit and the SD-5A014-01 peripheral processor interface circuit. In addition to these modified processor units, the communication bus circuit SD-1A119 must also be modified to provide maintenance of the peripheral unit bus and to improve maintenance of the peripheral addressing system.◆

FIRMWARE UPDATING

4.09 Firmware used in the PUC consists of software programmed into erasable programmable read only memory (EPROM). The EPROM consists of integrated circuits mounted on circuit packs installed in the PUC frame. It has the capability of being erased and reprogrammed when a program change occurs.

4.10 The prompt remotely operated memory update system (PROMUS*) is used to reprogram the PUC firmware. The PROMUS unit has the capability to erase, reprogram, and verify EPROM.

4.11 A basic PROMUS unit is capable of simultaneously programming two circuit packs and erasing one. The basic unit can be expanded by adding programming and erase modules to program a total of eight and to erase a total of six circuit packs.

4.12 The PROMUS units are located at centralized programming sites where the circuits are reprogrammed and shipped to the telephone company.

4.13 The update process begins with an information-only broadcast warning message (BWM)

*Trademark

sent over the software change administration and notification system (SCANS). The appropriate circuit packs are then reprogrammed and shipped.

5. DIGITAL CARRIER TRUNK APPLICATION

5.01 The PUC/DCT application (Fig. 6) provides call processing and channel multiplexing for up to 480 T1-channels (24 channels in each of 20 digroups) per DCT frame. The PUC is mounted in the center bay of a three-bay DCT frame. Shelf locations and circuit pack FG numbers are indicated in Fig. 7. Voltage regulators and power distribution units are mounted on the right-hand side of the shelves. The power and alarm control unit is located directly under controller 0 on a separate panel. Levels 66 and 74 slots 20 through 29 are special application circuit packs for DCT. One FG67 circuit pack is required for each digroup appearing in the DCT frame. The DCT application firmware resides in the CPU hardcore.

5.02 The DCT application firmware resides in the controller memory in the form of ROM. There are several PUC functions associated with the DCT application firmware. These functions include interfacing the No. 1/1A ESS CC with digroups and combined channel units (CCU), directing changes in signaling states, and summarizing and reporting changes in supervisory states. The PUC generates and receives dial pulse digits and revertive pulse digits.

5.03 ◆The active PUC controller receives and translates relatively high-level CC orders into primitive control signals necessary to interface with the wired-logic digroup controllers.◆ Call processing orders for the PUC/DCT are loaded in standard ESS peripheral order buffers (POBs). The orders are sent from the ESS to the PUC/DCT frame over the PUAB. The orders are in the form of 23-bit words. The orders are stored in a first in-first out buffer until the PUC's microprocessors are ready to execute them. This first in-first out buffer is called a data input first in-first out buffer (DIF). A DIF controller (DIFC) is used to control the loading and unloading of the buffer.

5.04 ◆The SCAM has a 64-row and 16-column scanner configuration. The DCT application uses two scanners.

5.05 The PUC circuit unique to the DCT application is called a digroup buffer circuit (Fig. 7). This circuit consists of two 32-word FIFO buffers.

The words consist of eight data bits and one even parity indicator. One FIFO buffer for input and the other is used for output. The input FIFO buffer stores orders and data destined for the digroup controller in the channel bank. The output FIFO buffer stores data concerning trunk and digroup controller states. One digroup buffer is required for each digroup equipped.◆

5.06 The DCT program cycle (Fig. 8) operates on a 10 millisecond interrupt from a clock. After initialization, the change reports from the digroup buffers are processed. The program then unloads an order from the FIFO buffer to load it into a hopper in the RAM. The BELLMAC-8 microprocessor decodes the order type, stores the order in the proper hopper for execution and sets an execution flag. The program terminates unloading of the FIFO buffer if the hoppers fill or if a high priority PUC maintenance order is found.

5.07 If there is a maintenance order which requires reconfiguration, the program will stop execution until the next program cycle. If there are no maintenance orders or they are low priority, the program continues. Timing list execution involves processing the information in each pulsing state register (PSR) on the list.

5.08 Executing orders on trunks involves processing state changes from ESS POB orders, checking the consistency of the states, and changing the state of the CCU. Orders to assign or release a link between a PSR and an ESS call register may also be executed. The program may also process digit output orders for outgoing calls on dial pulse or revertive pulse trunks. The program now services digroup buffers again until a necessary real time break for timing or output occurs. If there is enough time remaining, some background work may be done. This includes circuit diagnostics, data structure audits, translation updates from the ESS, and carrier facility monitoring (error rate counts). The program will start over when the 10 millisecond interrupt occurs.

5.09 The DCT firmware programs provide the capability of receiving, interpreting, and executing trunk state control and signaling orders from the ESS central control. In addition, it will process supervision and signaling (dial pulse, revertive pulse, and multifrequency) based on information from the digroup controllers. The programs also contain audits to keep all the data structure sane and intact.

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```
        TRUNK      TRUNK                                DIGITAL       MAIN
        LINK    DISTRIBUTING                         CROSS-CONNECT DISTRIBUTING
       NETWORK     FRAME                                 FRAME        FRAME

                                        COMBINED
                                        CHANNEL
                                         UNITS
                                                    DIGITAL
                                                    CARRIER
                              48 CIRCUITS           TRUNK
                                                    BANK
                                        COMBINED
                                        CHANNEL
                                         UNITS



                                                              RANDOM
                          FIRST                               ACCESS
      PERIPHERAL          IN-                                 MEMORY
        UNIT             FIRST          MICROPROCESSORS
      ADDRESS             OUT                                READ ONLY
        BUS             BUFFER                                MEMORY



                                        100
       CENTRAL                       MILLISECOND    MESSAGE
       CONTROL                       SUPERVISORY    BUFFER
      PROCESSOR                         SCAN
       COMPLEX
                     PERIPHERAL UNIT
                      ADDRESS BUS


                     SCANNER ANSWER BUS
```

Fig. 6—Peripheral Unit Controller/Digital Carrier Trunk Block Diagram

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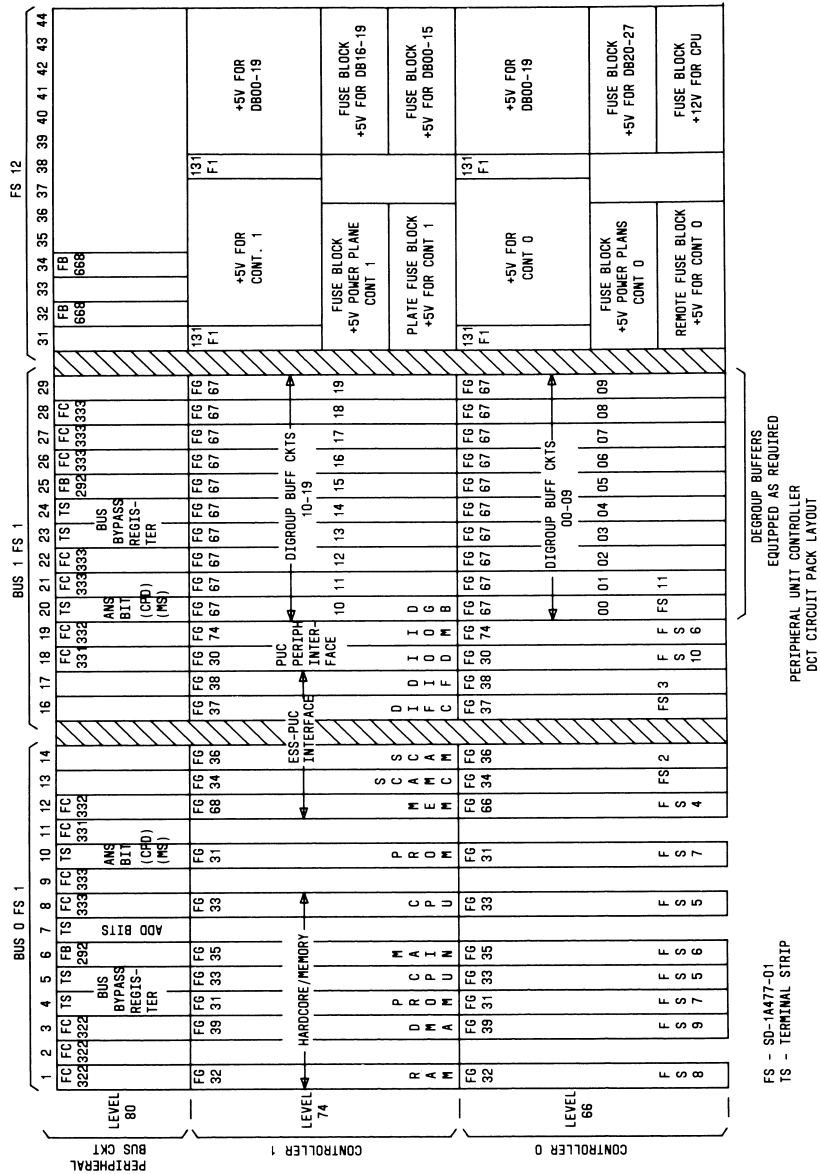
Fig. 7—Peripheral Unit Controller—Digital Carrier Trunk Circuit Pack Layout

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```
        ┌──────────────────────────┐
        │  10 MILLISECOND INTERRUPT │
        └──────────────────────────┘
                     │
        ┌──────────────────────────┐
        │      INITIALIZATION       │
        └──────────────────────────┘
                     │
        ┌──────────────────────────┐
        │  SERVICE DIGROUP BUFFERS  │
        └──────────────────────────┘
                     │
        ┌──────────────────────────┐
        │  UNLOAD FIRST IN-FIRST    │
        │        OUT BUFFER         │
        └──────────────────────────┘
                     │
              ╱ MAINTENANCE ╲
        YES  ╱   ORDERS?     ╲  NO
```

Fig. 8—Peripheral Unit Controller Program Cycle for Digital Carrier Trunk

The firmware consists of a main program, modules called directly by the main, and subroutine modules. The main program initializes the program cycle when it is entered.

DATA STRUCTURES

5.10 Data structures are blocks of memory used by the DCT firmware programs to store and retrieve data for various operations. Some of the data structures are in RAM where data may be stored. Other data structures are in ROM where data can only be read.

A. Digroup Register

5.11 Each DCT digroup has one digroup register (DR) assigned to it. This register occupies 16 eight-bit bytes of the SCAM in a fixed location. The data in this register is used to keep track of the digroup error history and maintain a communication link with the combined channel units (CCUs) plugged into the digroup. The DR contains the message being processed from the digroup buffer circuit, status and alarm bits, and error counts.

B. Trunk Register

5.12 There is one trunk register (TR) for each CCU. Each TR occupies 4 eight-bit bytes of SCAM. The first byte of the TR contains the trunk status. The second byte contains ordered trunk state changes which have not been completed and process markers which indicate that a trunk state change was detected and is being procesed. The third byte contains translation data for the trunk which gets pumped up periodically by the ESS. The fourth byte contains either a link to a PSR or a progress marker when the trunk is active on a call. When the BELLMAC-8 microprocessor receives an order from a POB, the TR is checked to see if it is a valid order.

C. Pulsing State Register

5.13 The PSRs are used for storing and processing data on trunks which are in the transient state. The PSR is attached to the TR during digit pulsing. These registers are used for timing and counting dial pulses and revertive pulses. They are also used for wink detection on operator trunks. The PSR contains the digits received from or to be transmitted to the connected office, the link index to the ESS call register, and address pointers to timing

lists. The PSR also contains the trunk state ordered by the ESS and the state of current PSR activity. Each PSR uses 22 eight-bit bytes of memory.

D. Timing Structures

5.14 Each timing list has a four-byte headcell which forms the pointers to the first and last registers on that particular list. There are three types of timing lists which are relatively short, medium, or long in time.

E. Order Hopper

5.15 The order hopper receives the orders read out by the FIFO buffer. All of the orders in the FIFO buffer are unloaded during each 10 millisecond program cycle. The order hopper provides for four POB orders and eleven non-POB orders. Only four POB orders can come in during one cycle, so there is no possibility of overflow. If more than eleven non-POB orders are received, the firmware program will begin executing the orders starting with the POB orders first.

F. Link Table

5.16 The link table serves as a translator to convert the link number used by the ESS call processing programs to a PSR number. The PSR number is an index into the memory blocks of PSRs.

G. Firmware Counts

5.17 Firmware counts are maintained on various events which indicate the status of the PUC. For example, counts are kept on the number of times a TR audit completed and the number of times that the PUC failed to seize a PSR at a time that one was required. These counts are kept in a 32-byte dedicated memory block. The ESS CC can request that the counts be reported through the message buffer upon demand. The CC is responsible for getting the counts out of the PUC and for resetting them.
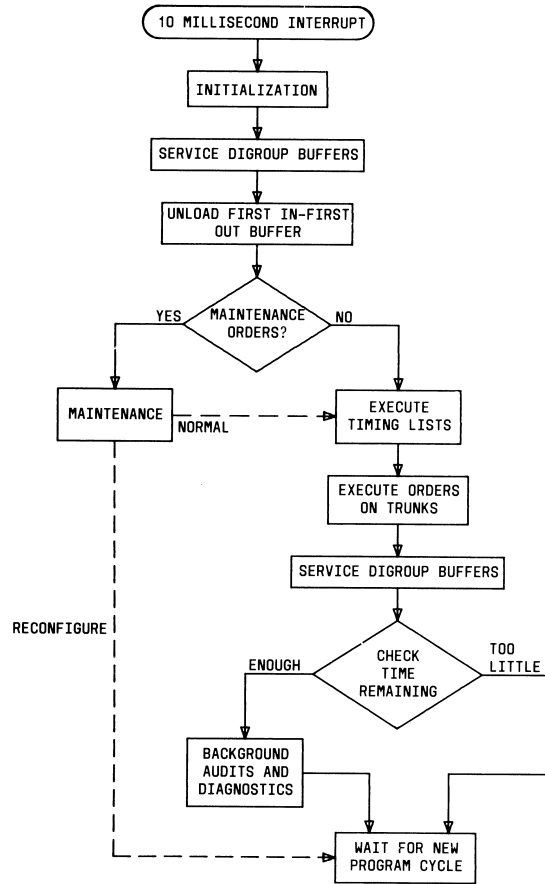
H. Parameters

5.18 The PUC application program for DCT requires parameters to do certain types of timing. These parameters are pumped up from the CC periodically. They are stored in a dedicated memory block named PARAM. This memory block is 16 bytes long.

I. Digroup Buffers in Service

5.19 The PUC maintenance programs require an indication of which digroup buffer circuits are in service. This block of memory consists of three bytes with each bit (0-19) assigned to one digroup buffer circuit. If the circuit is in service, the bit is set to a one. Four bits are not used and must be zero.

J. Address Block

5.20 This block of memory contains the parameters used most frequently during a given call. The first two bytes of the address block hold the flag bits which indicate parameters in the block are present. The block includes such parameters as the trunk circuit number, internal trunk number, and pulsing state register number. The digroup, trunk, and PSR pointers are also included.

K. Conversion Tables for Trunk and Channel Numbers

5.21 The ESS refers to trunks numbered from 0-119, 128-247, 256-375, and 384-503. In each quadrant, the trunks are numbered in the order of their physical position in the channel banks. The internal representation of the channel numbers in the DCT uses the numbering scheme employed by the digroup controller unit. The first channel is 4, the last channel is 27, the increment from one channel to the next is 4, and the sequence wraps around when the next value would exceed 27. In order to provide a quick way to convert between the two numbering schemes, these tables, stored in ROM, are provided.

L. Conversion Tables for State Designations

5.22 These tables are provided to convert between the state designations used in orders from the central control and the designations employed by the channel bank hardware.

M. Miscellaneous Data Tables

5.23 These are tables of constants required for miscellaneous functions in the DCT operational programs.

INPUT FORMAT

5.24 Peripheral order buffer orders from the ESS CC are sent over the PUAB and written into the FIFO buffer. The orders are in two general forms:

DCT application operational orders and DCT application maintenance orders.

5.25 The DCT input application operational orders all follow the general form shown in Fig. 9. These orders are distinguished from the maintenance orders by the maintenance order indicator in bit 17. This bit is always set to zero for DCT applicaton operational orders.

5.26 The general form of the DCT application maintenance order is shown in Fig. 10. A one in bit position 17 indicates that the order is a maintenance order and not an operational order.

OUTPUT FORMAT

5.27 Messages from the PUC/DCT are unloaded from the SCAM and transmitted over the scanner answer bus to the ESS. These messages consist of 16-bit words called DCT application operational messages and DCT application maintenance messages.

5.28 The DCT output application operational orders follow the general form shown in Fig. 11. These messages are distinguished from maintenance messages by the maintenance indicator (bit position 15). This bit is zero for all operational messages.

5.29 The DCT application maintenance messages are in two forms, a single word message and a multiple word message. They are both 16-bit words with the maintenance indiator in bit position 15 set to a one. Figure 12 shows the general form of a single word maintenance message. Figure 13 gives the general form of the multiple word maintenance message.

DIGROUP ORDERS AND MESSAGES

5.30 Communication with the digroup controller unit (DCU) takes place over a serial channel implemented on the digroup buffer circuit pack. The serial channel is asynchronous at approximately 20,000 bits per second. The general format of the 8-bit data values exchanged between the PUC program and the digroup buffer/digroup controller is shown in Fig. 14.

6. DATA LINK APPLICATION

6.01 ◆The peripheral unit controller/data link (PUC/DL) is a particular application of the

PUC. It is designed to serve as a general purpose DL controller for several projects requiring a DL from ESS central office. The PUC/DL provides an interface between a No. 1/1A ESS central office and up to 16 bidirectional DLs. The RSS interface is described in Section 231-037-022. The ETS interface is described in Section 231-037-023. The CCIS interface is described in Section 231-037-025.

6.02 The PUC/DL feature is available with the 1E6 and later generic programs for No. 1 ESS and 1AE6 and later generic programs for No. 1A ESS. The PUC/DL feature is addressed in Section 231-090-062.◀

6.03 The PUC/DL application program receives and sends data to the CC and selects 1 of 16 possible DLs for transmission. The PUC is mounted in the top section of a single bay frame (Fig. 1). Shelf locations and circuit pack FG numbers are indicated in Fig. 15. The power and fuse unit is mounted below the PUC/DL unit. Directly below the power and fuse unit is the power and alarm control unit. Levels 66 and 74 slots 22 through 44 are special application cir-

cuit packs for DLs termed line interface units (LIUs). One LIU is required for each DL equipped. LIUs are different for the various DL applications. Data link application firmware resides in the controller memory in the form of ROM.

6.04 Data exchanged between the No. 1/1A ESS and PUC/DL consists of application information and maintenance information. The insertion and deletion of protocol words and any necessary error recovery actions are handled within the PUC/DL.

6.05 Communication from the ESS to the PUC/DL comes through the input FIFO buffer memory (Fig. 16). Three byte data words are read from the FIFO.

6.06 Data is passed to the ESS from the PUC/DL by writing it into the SCAM. The SCAM is a specified address range of the PUC/DLs' read/write memory. The ESS has read-only access to these locations where they are treated as a sequence of scanner rows. This data is passed over the SCAB. Data links are accessed through the I/O decoder.

BIT POSITIONS

22 21 20	19	18	17	16																	0
COM	*	D1	M									D2									

COM – COMMAND CODE. THIS THREE BIT FIELD
        SPECIFIES THE TYPE OF OPERATION REQUIRED
        BY THE ORDER.
        001 – STATE CHANGE ORDER FOR A TRUNK.
        010 – DIGIT OUT ORDER FOR OUTPULSING ON
        A TRUNK.
        011 – LINK ORDER FOR ASSOCIATING A LINK
        BETWEEN A PSR IN THE PUC AND AN ESS CALL
        REGISTER.
        101 – DETECT STPS (START PULSING SIGNAL)
        ORDER, USED TO INFORM THE PUC ABOUT
        START PULSING FOR A TRUNK.

D1 AND D2 – DATA ASSOCIATED WITH THE SPECIFIC ORDER
        TYPE INDICATED BY THE COMMAND CODE.

M – MAINTENANCE ORDER INDICATOR. THIS BIT
        IS ALWAYS ZERO FOR DCT OPERATIONAL ORDERS.

* – THIS BIT IS NOT USED. IT MUST BE ZERO DUE
        TO INTERACTIONS WITH CERTAIN ESS PROGRAMS.

Fig. 9—Digital Carrier Trunk Input Operational Orders, General Form

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```
                              BIT POSITIONS
     22 21 20 19 18 17 16 15                             0
    |PR|AP| HOP  |M |L |              DATA                 |
```
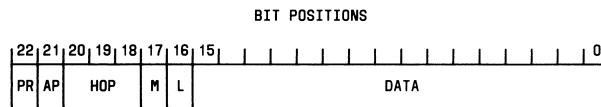
```
     PR – PRIORITY INDICATOR. MUST EQUAL O (LOW
          PRIORITY) FOR APPLICATION MAINTENANCE
          ORDERS.
     AP – APPLICATION ORDER INDICATOR FOR LOW
          PRIORITY MAINTENANCE ORDERS.
    HOP – THE HIGH ORDER 3 BITS OF THE OPERATION CODE
          OF THE ORDER.
      M – MAINTENANCE ORDER INDICATOR. A ONE IN
          THIS BIT POSITION ALWAYS OCCURS FOR
          MAINTENANCE ORDERS.
      L – THE LOW ORDER BIT OF THE OPERATION CODE OF
          THE ORDER.
   DATA – THE DATA ASSOCIATED WITH THE PARTICULAR
          ORDER TYPE INDICATED BY THE OPERATION CODE.
```

Fig. 10—Digital Carrier Trunk Input Maintenance Order, General Form

```
                              BIT POSITIONS
       15 14 13 12 11                    0
      |M |  MT  |          DATA           |
```
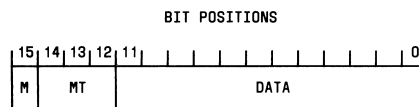
```
      M – MAINTENANCE INDICATOR. THIS BIT IS O FOR ALL
          APPLICATION OPERATIONAL MESSAGES.

     MT – MESSAGE TYPE INDICATOR.
          OO1 – DIGIT RECEIVED MESSAGE.
          O1O – TERMINATING REVERTIVE PULSE REPORT
                MESSAGE.
          O11 – SXS FAST RESEIZURE MESSAGE.
          1OO – SXS PREPULSE MESSAGE.
          11O – WINK DETECTED MESSAGE FOR INBAND OPERATOR
                TRUNK SIGNALING.
          111 – GENERAL REPLY MESSAGE.

   DATA – DATA DEPENDING ON THE MESSAGE TYPE.
```

Fig. 11—Digital Carrier Trunk Output Operational Messages, General Form

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BIT POSITIONS

```
 15  14  13  12                               0
|   |   |   |   |   |   |   |   |   |   |   |   |
| M | MW| P |              DATA                 |
```
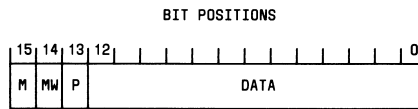
M – MAINTENANCE INDICATOR. THIS BIT IS ONE FOR ALL
     MAINTENANCE MESSAGES.

MX – MULTI-WORD MESSAGE INDICATOR. THIS BIT IS
     ZERO FOR SINGLE WORD MESSAGES.

P – PUC MESSAGE INDICATOR. THIS BIT IS ZERO FOR
     APPLICATION MAINTENANCE MESSAGES.

DATA – THE CONTENTS OF THIS 13 BIT FIELD ARE
       THE DATA FOR THE MESSAGE.

Fig. 12—Single Word Digital Carrier Trunk Output Maintenance Message, General Form

BIT POSITIONS

```
 15  14  13  12  11  10  9   8   7                 0
|   |   |   |   |   |   |   |   |   |   |   |   |   |
| M | MW| P | * |      LN     |        TY          |  ◄— HEADER WORD
|                                                  |  ◄— DATA WORD(S)
```
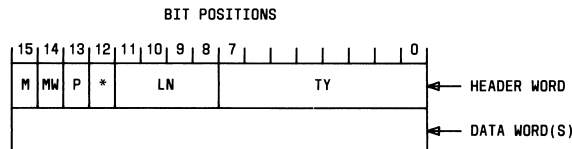
M – MAINTENANCE MESSAGE INDICATOR. THIS BIT WILL BE
     ONE FOR ALL MESSAGES IN THIS CLASS.

MW – MULTI-WORD MESSAGE INDICATOR. THIS BIT WILL
     BE ONE FOR ALL MESSAGES IN THIS CLASS.

P – PUC MESSAGE INDICATOR. THIS BIT WILL BE
     ZERO FOR ALL MESSAGES IN THIS CLASS, SINCE
     THEY ARE ALL APPLICATION MAINTENANCE MESSAGES.

LN – THE LENGTH INDICATOR. THE VALUE OF LN WILL
     BE TWO LESS THAN THE TOTAL MESSAGE LENGTH
     INCLUDING THE HEADER.

TY – TYPE. THIS EIGHT BIT FIELD SPECIFIES THE
     TYPE OF MESSAGE.

* – THIS BIT IS NOT ASSIGNED.

Fig. 13—Multiple Word Digital Carrier Trunk Output Maintenance Message, General Form

```
                          BIT POSITIONS

                    7 | 6 |   |   | 2 | 1 | 0
                   +---+-----------+---------+
                   | X |  ADDRESS  |   YZ    |
                   +---+-----------+---------+
```

X – A CONTROL BIT USED TO SPECIFY ONE OF TWO
    CLASSES OF ORDERS OR MESSAGES.

ADDRESS – THIS FIVE BIT FIELD NORMALLY CONTAINS
    A CHANNEL ADDRESS, WHICH IS A VALUE IN
    THE RANGE 00100 THROUGH 11011. IF THE
    VALUE IS NOT IN THAT RANGE, A SPECIAL
    FUNCTION SPECIFIED BY THE OUT-OF-RANGE
    (OOR) CODE IS PERFORMED.

YZ – THIS FIELD CONTAINS EITHER DATA
    CORRESPONDING TO A PARTICULAR CHANNEL,
    A CODE SPECIFYING WHAT DATA IS BEING
    REFERENCED BY THE ORDER OR MESSAGE, OR
    DATA CORRESPONDING TO THE ENTIRE DIGROUP.

Fig. 14—Digital Carrier Trunk Digroup Order and Message, General Form

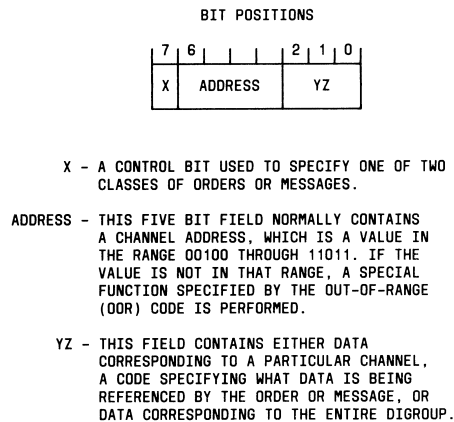**6.07** The PUC/DL firmware consists of common routines and protocol blocks (Fig. 17). Common routines can be used with different types of DLs. They are involved in functions such as the input of data, timing, and audits. The link dependent operations are taken care of within the protocol blocks. A protocol block is a group of subroutines designed to take data from a buffer in memory and dispatch it on a link following the rules of a specific DL protocol. The maintenance functions for the link interface hardware are also included in the protocol blocks.

COMMON ROUTINES

A. Timing

6.08 A 20-millisecond software clock is maintained for timing. The clock has a 16-bit output and a single client delayed entry is provided.

B. Input

6.09 All incoming data from the ESS is read from the input FIFO buffer and sorted in three categories—data, parameters, and maintenance orders. The data is destined to be sent on a DL. Data is not addressed to a specific link number; it is marked with a destination number specifying a buffer in the PUC/DL read-write memory. One destination buffer exists for each remote terminal. The association of a destination buffer and a single data link is specified in a parameter. Switching between redundant links can be requested through a maintenance order. The switching can occur during communication without loss of data.

6.10 Incoming data is placed in the destination buffer requested in the data heading (first) word. This buffer is managed as a linked list. See Fig. 18. Each new message is added to the end of the list. The buffer is circular, thus the physical end of the address space is of no concern. When the buffer is full, as indicated when the end of the list meets the beginning, the present data message is discarded and an error reported. This action is necessary to prevent one link out of service from jamming all data flow through a PUC/DL. Such a problem would otherwise occur since there is no way to look ahead in the input FIFO buffer other than to read the bottom message and either store or discard it. Cumulative counts are kept of all words unloaded from the FIFO buffer and from the destination buffers. These counts are recorded in the SCAM where they are read and used by the ESS to control the input rates and prevent overflow in normal operation.

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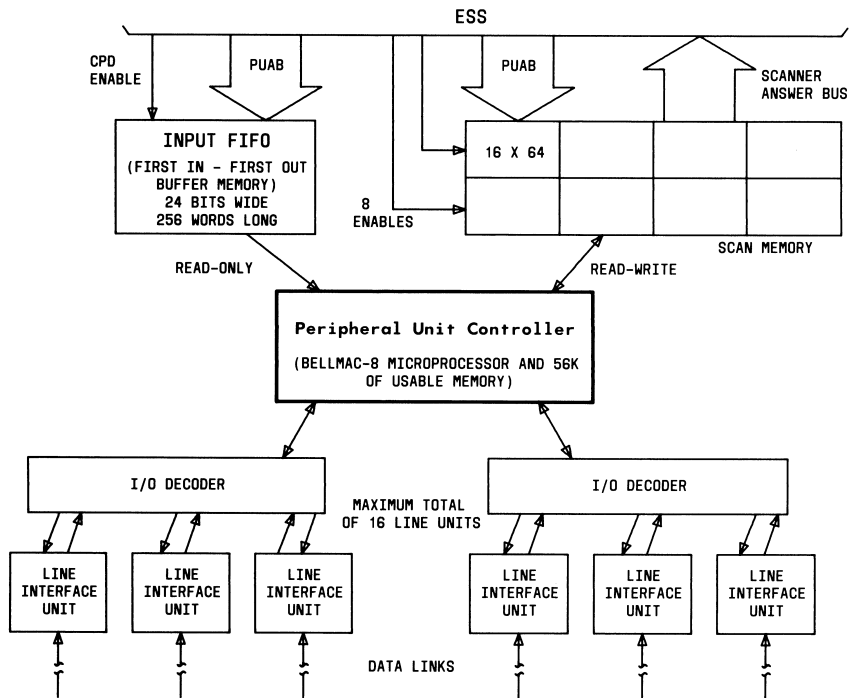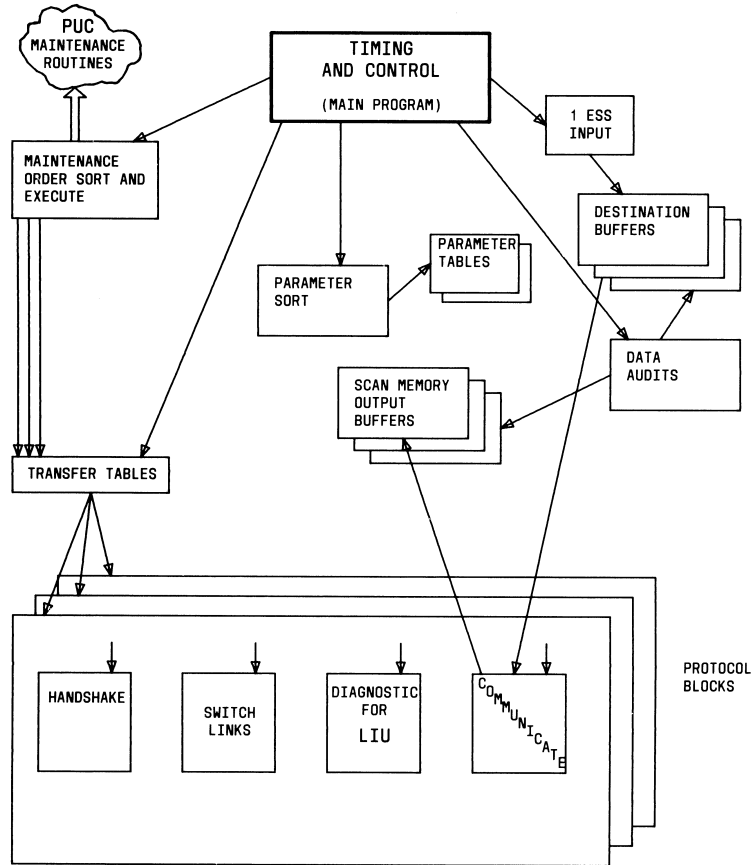

Fig. 15—Peripheral Unit Controller—DL Circuit Pack Layout

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Fig. 16—Peripheral Unit Controller/Data Link Block Diagram

Fig. 17—Peripheral Unit Controller/Data Link Firmware Structure Simplified

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```
POINTERS IN BUFFER                          BUFFER DATA AREA
CONTROL AREA

    ┌──────────────┐          ┌──────────────────┐
    │              │─────────▶│  LINKAGE WORD     │
    └──────────────┘          │  ────────────     │
    "BOTTOM" THE OLDEST       │                   │
    MESSAGE ON THE LIST       │  DATA - ANY LENGTH │
                              │  ────────────     │
                              │  LINKAGE WORD     │
                              │  ────────────     │
                              │     DATA          │
                              │  ────────────     │
                              │  LINKAGE WORD     │
                              │  ────────────     │
                              │     DATA          │
                              │  ────────────     │
    ┌──────────────┐          │     EMPTY         │
    │              │─────────▶│  ────────────     │
    └──────────────┘          │  ────────────     │
    "TOP" THE MESSAGE         │  ────────────     │
    NOW BEING RECEIVED        │  ────────────     │
                              │                   │
    ┌──────────────┐          │                   │
    │              │─────────▶│                   │
    └──────────────┘          └──────────────────┘
    "LOAD" THE NEXT WORD
    RECEIVED WILL BE STORED HERE
```
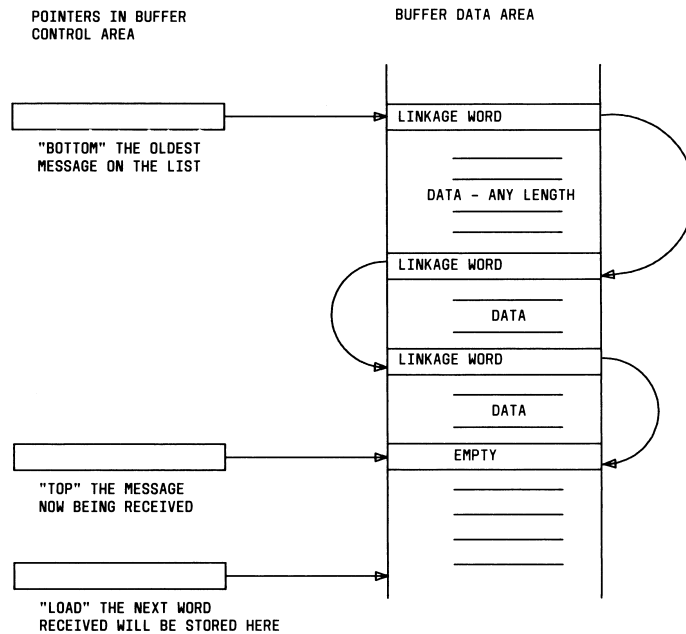
Fig. 18—Peripheral Unit Controller/Data Links Destination Buffer Structure

6.11 The PUC/DL operation is defined by parameter input messages. Most parameters are sent when the unit is brought on-line. Receipt of a parameter causes a table entry to be initialized or changed and an audit request generated. The audit routine will be run at the next opportunity. It alters the internal data structures to agree with the new parameter. Parameters specify things such as the number and length of destination buffers, the number, length, and location of data output buffers in the SCAM, or the destination and protocol type of each DL.

6.12 The PUC maintenance orders are split off immediately. These are processed by the controller maintenance programs and are of no concern to the application firmware. Application maintenance orders are what remain. They initiate func-tions such as bringing a DL on-line, clearing an error count, or switching between redundant DLs to the same destination.

C. Audits

6.13 The main purpose of audits is to build and initialize data structures in the read/write memory. The input for all audits comes from the parameter table. The output is pointers which delimit data buffers. The audit routines are a run-time memory allocation facility. They provide space for destination buffers and scratch blocks when these areas are requested by parameter inputs. The entire sequence of audits are run whenever parameters are changed. Otherwise, they are a low priority background task providing recovery from errors.

PROTOCOL BLOCK ROUTINES

6.14   The duties of a protocol block are to take data from a destination buffer and send it over a data link and to take data from the link and record it in the SCAM. The protocol block includes whatever routines are necessary to implement a protocol handshake and a transfer of communication to a standby link without loss of data. The diagnostic programs for the LIU are considered part of a protocol block although they may be shared between protocols using the same DL interface hardware.

A.   Communicate

6.15   The first action is to empty the LIU receiver FIFO buffer. If the resulting words complete a data link frame, a reply is assembled and sent. There is a separate receive subroutine for each of the seven data frame types. These carry out the actions pertinent to that message and reply by selecting the appropriate send subroutine. There are send subroutines for all frame types except "receiver not ready." This response is never required since it is assumed that the ESS input routine will never let the SCAM buffers overflow; thus the PUC/DL is always ready for another message. The SCAM buffers are circular. Each is provided with a load pointer, updated by the protocol routines, when a data frame is received error-free. The pointer specifies where the ESS input routine is to stop reading.

6.16   Data is transmitted when two conditions are met. There must be room for an entire data frame in the LIU send FIFO buffer and the destination buffer associated with this link must have data ready to send. When this is true, one frame will be sent. It will carry a maximum of 16 data bytes.

B.   Handshake

6.17   The handshake function is called whenever an order is processed to make a link active. The protocol block subroutine is selected by reference to the protocol parameter for the link specified in the maintenance message. The handshake routine resets all protocol variables and attempts to initialize communication by sending a set asynchronous response mode data link frame. If the handshake is successfully answered, a link-restored message is returned to the ESS. If the handshake does not complete properly, a protocol impasse report is returned to the ESS. This indicates that either the link or the remote end device is inoperative. A portion of the code which initializes certain variables is called when processing a clear destination buffer maintenance message. This prevents generating confused output if the buffer is cleared when sending is active.

C.   Switch Links

6.18   This protocol block is specific to applications using standby links. It comes as a response to a maintenance order requesting a soft (no data loss) switch to a standby link. A switch request is set pending until the data exchange is at a point where the switch can be accomplished with no loss or repetition of data. The protocol routines then alter the link status, setting the present link out of service and making the standby link active.

D.   Line Interface Units Diagnostics

6.19   The LIU diagnostics come as time permits near the end of a program cycle. The common routines record the arrival of a diagnostic request application maintenance message. When time is available, the diagnostic is run in segments. There may be any number of segments but each segment must take no longer than 3 milliseconds to complete. Diagnostic routines return a pass/fail report accompanied by two bytes of data. The interpretation of the data varies according to what is being tested. Separate LIU diagnostics are provided to locate a faulty circuit pack and to make an error rate check on a DL. Diagnostics are run only on inactive links.

PROGRAM TIME SEQUENCE

6.20   All application firmware activities are based on a 20-millisecond main program cycle (Fig. 19). This cycle time is enforced by a hardware timer. At the beginning of the cycle this timer is initialized and set running. Twenty milliseconds later the timer generates an interrupt, bringing control back to the start of the cycle and causing the sequence to repeat. If all goes well, all tasks scheduled will be completed and the processor will have halted (the wait state) when the timer interrupt occurs. If it is found still running, an error has presumably occurred placing the routine in a long or unending loop. In such an event, the next cycle is dedicated to running audits, which hopefully will remedy the difficulty. These actions occupy the initialize cycle block in the diagram.
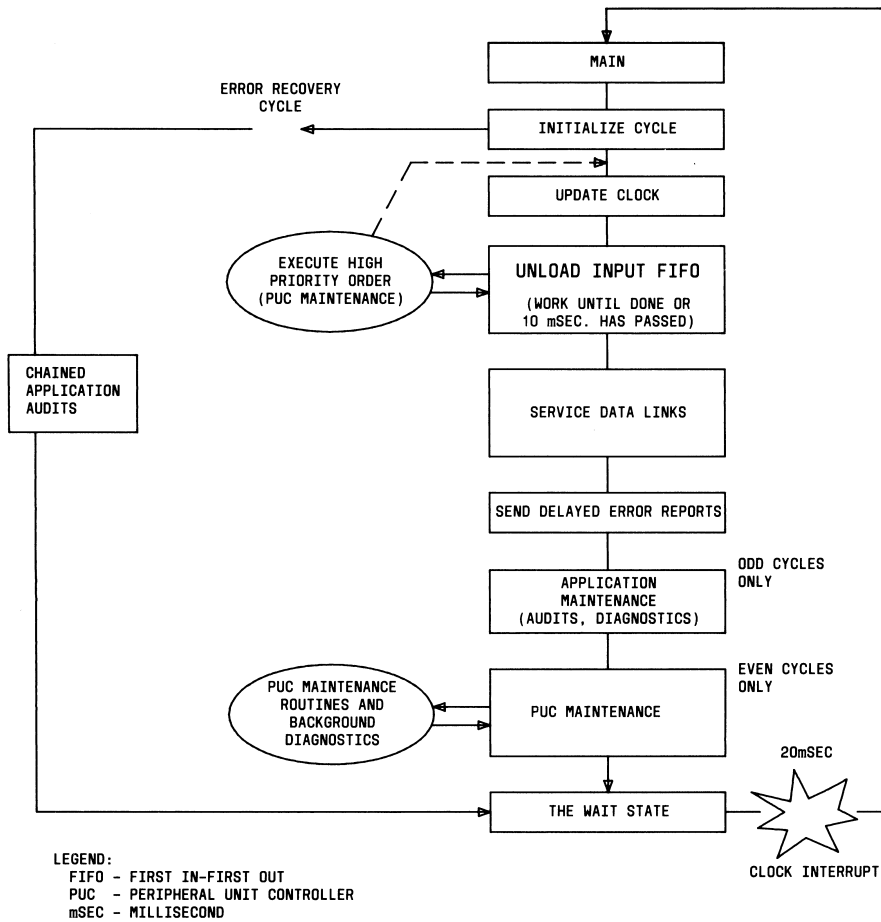
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```
                                    ┌──────────────────┐
                                    │       MAIN       │◄─────────────┐
                                    └──────────────────┘              │
ERROR RECOVERY                      ┌──────────────────┐              │
    CYCLE                 ◄─────────│ INITIALIZE CYCLE │              │
                            ┌ ─ ─ ─ └──────────────────┘              │
                            │       ┌──────────────────┐              │
                            │       │   UPDATE CLOCK   │◄─────┐       │
              ╱───────────╲ │       └──────────────────┘      │       │
             ╱  EXECUTE HIGH╲│       ┌──────────────────┐      │       │
            (  PRIORITY ORDER )◄─────│ UNLOAD INPUT FIFO│      │       │
             ╲(PUC MAINTENANCE)╱─────►│                  │      │       │
              ╲───────────╱          │ (WORK UNTIL DONE OR│    │       │
                                     │ 10 mSEC. HAS PASSED)│   │       │
                                     └──────────────────┘      │       │
┌──────────┐                        ┌──────────────────┐       │       │
│ CHAINED  │                        │                  │       │       │
│APPLICATION│                       │ SERVICE DATA LINKS│      │       │
│ AUDITS   │                        │                  │       │       │
└──────────┘                        └──────────────────┘       │       │
                                    ┌──────────────────┐        │      │
                                    │SEND DELAYED ERROR REPORTS│  │     │
                                    └──────────────────┘        │      │
                                    ┌──────────────────┐  ODD CYCLES   │
                                    │   APPLICATION    │  ONLY         │
                                    │   MAINTENANCE    │               │
                                    │(AUDITS, DIAGNOSTICS)│            │
                                    └──────────────────┘               │
              ╱───────────╲         ┌──────────────────┐ EVEN CYCLES   │
             ╱PUC MAINTENANCE╲      │                  │ ONLY          │
            ( ROUTINES AND    )◄────│  PUC MAINTENANCE │               │
             ╲ BACKGROUND     ╱────►│                  │               │
              ╲ DIAGNOSTICS  ╱      └──────────────────┘               │
              ╲───────────╱                                20mSEC      │
                                    ┌──────────────────┐               │
                              ─────►│  THE WAIT STATE  │──────✦────────┘
                                    └──────────────────┘
                                                       CLOCK INTERRUPT
```

LEGEND:
  FIFO – FIRST IN-FIRST OUT
  PUC – PERIPHERAL UNIT CONTROLLER
  mSEC – MILLISECOND

Fig. 19—Peripheal Unit Controller/Data Link Main Program Cycle

6.21   The main program itself is mostly a series of subroutine calls. After initialization, the next routine called unloads the ESS input FIFO buffer. The input words are read and sorted. Data words are deposited in destination buffers. Application maintenance orders involving little processing are executed at once. Others are recorded for attention later in the cycle. Parameters are written into the parameter table. When a parameter is received, the audit cycle is restored to the beginning and audits are increased in priority. The PUC maintenance orders are sorted by priority. High priority orders are executed as they are received with a call to a PUC maintenance program. Low priority orders are stored. They will be executed when time permits at the end of the cycle. As words are removed from the FIFO buffer, the unload word count is advanced. This is a word in the SCAM needed by the ESS output programs to keep record of empty words and prevent overflowing the FIFO buffer. Unloading terminates when the FIFO buffer is found empty or after 10 milliseconds have been spent in this task.

6.22   Control then passes to the DL service routine whose responsibility is to locate the active DL and run the communicate section of their corresponding protocol blocks. The active indicator is a bit in the parameter table. This table is searched in numerical sequence. When an active link is found, its protocol number is retrieved and control is given to the specified protocol block. When its activity completes, the search is resumed, finding the next active link. Data link service terminates when 16 links have been serviced or if less than 5 milliseconds remain in the program cycle. This implies that a protocol block communicate entry must always complete in less than 5 milliseconds. When DL service is resumed in the next program cycle, the search for active links will start where it left off. Thus, high-numbered links will not receive nonuniformly degraded service as the communication load increases.

6.23   The next action will not usually occur. A delayed error report is sent only in cases where an error report was suppressed because the SCAM maintenance output buffer was full when the report was generated.

6.24   When DL service has completed, the hardware clock is read. If less than 3 milliseconds remain in the present cycle, no more tasks are entered and the processor is halted. If enough time remains, maintenance routines are run. This service alternates between PUC maintenance and application maintenance. If the cycle number, as read from the software clock is even, control is given to the PUC maintenance routines. If a low priority PUC maintenance order has been received, it is executed at this time. Otherwise, background diagnostics are called. When the cycle count is odd, application maintenance runs. This task is either an audit segment or executing a deferred application maintenance order. If a parameter has been received since a complete cycle of audit segments has run, the next audit segment receives control, regardless of pending maintenance orders. If this is not the case, the choice is between a deferred order and an audit segment. If a deferred order exists, it is executed. This could be a request to make a DL active or an LIU diagnostic request. Either results in a call to a protocol block routine. When no such order is waiting, the application maintenance time is given to the next audit segment.

6.25   After completing PUC or application maintenance routines, the cycle is terminated. An indicator is set marking that the cycle was successfully completed. The processor then halts. When the 20-millisecond hardware timer expires, a new cycle will begin.
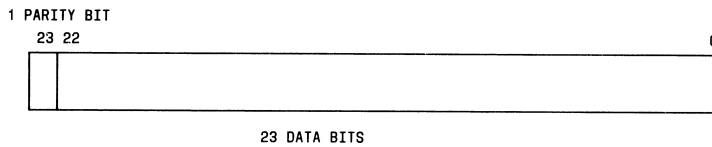
INPUT FORMAT

6.26   All application input to the PUC/DL enters through the input FIFO buffer. This first in-first out buffer is 256 words deep. It is completely a hardware function, providing time buffering of messages which is invisible to both the ESS and the PUC/DL software. Input to the FIFO buffer comes from the PUAB in short binary format. This supplies 23 bits of data plus one parity bit. The PUC/DL firmware interprets each such word as three 8-bit bytes. The application firmware recognizes the byte boundaries as delimiting message data fields (Fig. 20).

6.27   The first sort is on the basis of the leftmost byte of the input heading control field (Fig. 21). If the parity is incorrect (it should be odd), the word is discarded and an error report returned to the ESS. The next separation is governed by the maintenance/data bit. Data messages have a zero in this position.
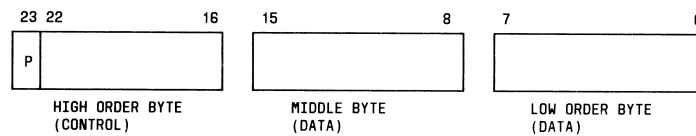
A.   Data Messages

6.28   A data message must begin with a heading, a word with only the application bit in the left

1 PARITY BIT

```
    23 22                                                    0
   ┌──┬──────────────────────────────────────────────────┐
   │  │                                                  │
   └──┴──────────────────────────────────────────────────┘
```

23 DATA BITS

SHORT BINARY WORD AS SENT BY NO. 1 ELECTRONIC SWITCHING SYSTEM

```
   23 22        16   15        8    7          0
   ┌─┬─────────────┐ ┌───────────┐ ┌────────────┐
   │P│             │ │           │ │            │
   └─┴─────────────┘ └───────────┘ └────────────┘
   HIGH ORDER BYTE    MIDDLE BYTE    LOW ORDER BYTE
   (CONTROL)          (DATA)         (DATA)
```

THE SAME WORD AS INTERPRETED BY THE PERIPHERAL UNIT CONTROLLER FOR DATA LINKS

Fig. 20—Peripheral Unit Controller/Data Link Input Format

byte set. Any word with zero in the maintenance bit and one or more nonzero data bits in the left byte will be interpreted as a data message heading (Fig. 22). The middle field of the heading contains the destination number. This specifies the transmit (destination) buffer where the words following will be stored. The heading is interpreted by the PUC/DL and discarded. It is never put in a destination buffer and therefore will not appear in a DL message. The right (low order) byte of the data message heading contains a word count. This is for error checking and must include the heading. This is a count of 24-bit ESS words written into the FIFO buffer. It is not a data link byte count. A data message having an incorrect word count will be discarded and an error reported.

6.29 The data words following the heading are identified by all data bits zero in the left byte. The low order two bytes will be placed in the destination buffer. They may be transparent data or protocol level control, depending on the protocol being used.

B. Maintenance Messages

6.30 A one in the maintenance bit marks a nondata message (Fig. 21). Such an item is always a one-word unit, never accompanied by data words. The next division in the category of maintenance messages separates application and PUC orders. This is sorted bit 22, which is one for application maintenance orders.

6.31 Application maintenance messages perform a variety of functions. All orders to activate and reconfigure data links are of this type, as are the messages which present and update parameters. Each application maintenance message is discussed in detail in the following sections.

OUTPUT FORMAT

6.32 Output of all data and control information is passed through the SCAM from the PUC/DL to the ESS. Output is of three types, incoming DL messages, error and status reports, and special indi-
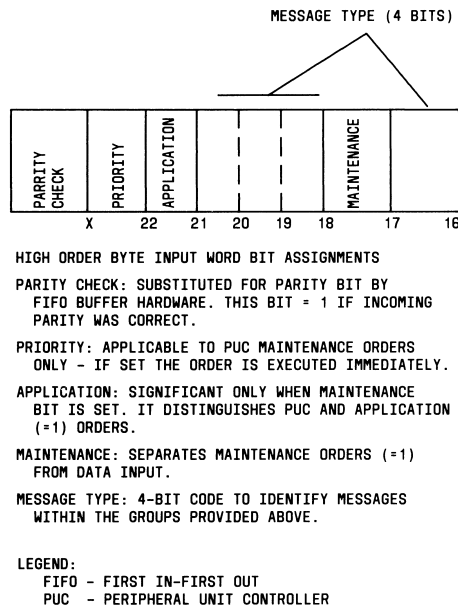
MESSAGE TYPE (4 BITS)

```
            PARITY   PRIORITY  APPLICATION              MAINTENANCE
            CHECK
             X        22        21    20   19   18       17    16
```

HIGH ORDER BYTE INPUT WORD BIT ASSIGNMENTS

PARITY CHECK: SUBSTITUTED FOR PARITY BIT BY
  FIFO BUFFER HARDWARE. THIS BIT = 1 IF INCOMING
  PARITY WAS CORRECT.

PRIORITY: APPLICABLE TO PUC MAINTENANCE ORDERS
  ONLY - IF SET THE ORDER IS EXECUTED IMMEDIATELY.

APPLICATION: SIGNIFICANT ONLY WHEN MAINTENANCE
  BIT IS SET. IT DISTINGUISHES PUC AND APPLICATION
  (=1) ORDERS.

MAINTENANCE: SEPARATES MAINTENANCE ORDERS (=1)
  FROM DATA INPUT.

MESSAGE TYPE: 4-BIT CODE TO IDENTIFY MESSAGES
  WITHIN THE GROUPS PROVIDED ABOVE.

LEGEND:
    FIFO - FIRST IN-FIRST OUT
    PUC - PERIPHERAL UNIT CONTROLLER

Fig. 21—Input Heading Control Field

cators. The latter are items such as buffer load and unload counts. Figure 23 is a layout map of the SCAM.

A.   Incoming Data from Data Links

6.33   Incoming data is deposited in per-destination circular buffers in the SCAM. The length and position of these output buffers are specified in a parameter. There are certain restrictions placed on these values by the readout algorithm used in the ESS. Each data output buffer is provided with a load pointer, also located in the SCAM. This points to the location where the next word (as yet unreceived) is to be written. The output buffer unload pointer exists solely within the ESS. It is expected that the unload routine will always be able to keep up with the PUC/DL and never allow overwriting to occur.

B.   Maintenance Messages

6.34   Maintenance messages are all communication that does not originate at the far end of a DL. They are delivered in the general reply buffer, located in a different part of the SCAM. Maintenance messages are error reports and parameter acknowledgments. They are considered to be of lower urgency than incoming data. Thus the general reply buffer is provided with both a load and an unload pointer, both recorded in a dedicated word in SCAM. Maintenance messages are sent only when there is space available in the buffer. If one or more reports have been supressed because the buffer was full, a message to this effect will be sent when buffer space becomes free. The identity of the original reports is lost.

C.   Special Indicators

6.35   Several examples of the special indicator output type have just been mentioned. They are the data output buffer load pointers (arrayed in a table) and the general reply buffer load and unload pointers (combined in the general buffer control word). Other special words in the SCAM are the FIFO buffer unload count and the table of destination buffer unload counts. These are used to determine how many words are available in the input FIFO buffer and in each destination buffer. A special word is provided to indicate when a DL switch is in progress. This is necessary because only one link switch can be performed at a time.

PARAMETERS

6.36   Parameters are application maintenance messages bringing items of data to the PUC/DL as the controller is being brought into service. Their purpose is to tailor the PUC/DL memory allocation to the needs of the DL applications which it serves and to specify the characteristics of the individual DLs. Items such as the length of a transmit buffer or the type of protocol to be used on link number three are typical parameters.

6.37   All parameters are in the form of single word messages which communicate one byte of parameter information. The remaining two bytes of the input word are needed to distinguish the parameter from other types of messages and to specify which parameter is being communicated. The present layout of the parameter address space will accommodate
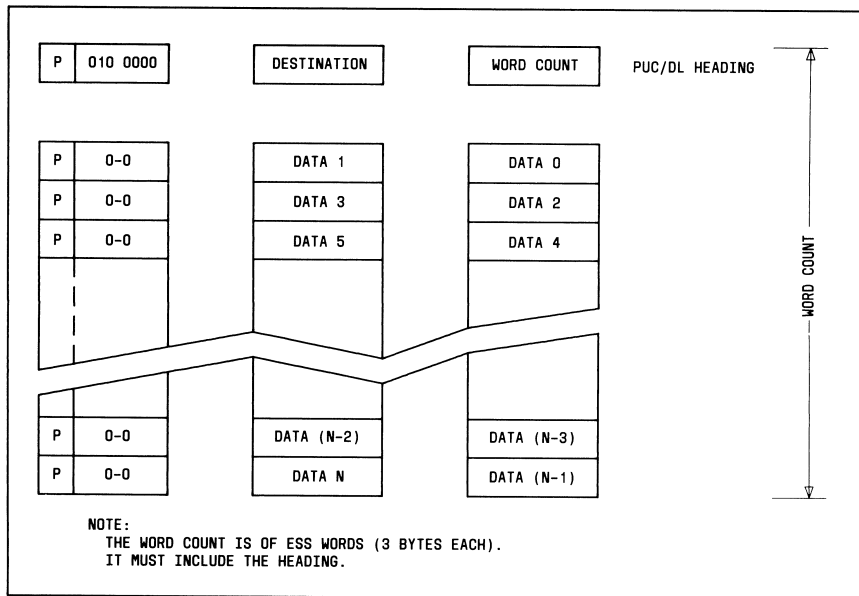
Fig. 22—Input Data Message

a total of 256 parameters. These parameters are subdivided into four categories. They are: general parameters, destination parameters, data link basic parameters, and data link protocol parameters. Figure 24 outlines the data fields in a typical parameter.

A.   General Parameters

6.38   The general parameters give information which is applicable to the operation of the entire PUC/DL. It is not specific to a particular DL, protocol, or destination. There are three general parameters. They are associated with the amount of RAM used, audit messages, and error messages.

6.39   A single data byte gives the number of 4000 word units of RAM installed in the PUC/DL. It can range from 1 to 12. When the PUC/DL is reset, this parameter will acquire the default value of 1, indicating that a minimum configuration exists.

When more memory than this is installed and is to to be used, this parameter must be updated before the parameters which cause memory to be allocated for the destination buffers. Failure to do this may result in a memory overflow failure message and cause the PUC/DL to drop all the destination buffers in excess of the memory limit. Setting the amount of memory to more than is actually present can prevent the PUC/DL from ever attaining a working configuration.

6.40   The parameter pertaining to audit messages can have the significant values of zero or not zero. If it is zero, all parameter responses and audit failure reports are suppressed. Otherwise, these messages are sent via the general reply buffer. The state of the audit message parameter can be changed at any time.

-ALL SCAM WORDS ARE 16 BITS WIDE-

SCAM 0

GENERAL (MAINTENANCE)
MESSAGE BUFFER

MESSAGE BUFFER CONTROL
FIFO UNLOAD CUMULATIVE COUNT
APPLICATION F-SCAN
(3 WORDS-NOT USED)
PUC F-SCAN
(3 WORDS)

SCAM 1

CUMULATIVE COUNTS OF WORDS
UNLOADED FROM DESTINATION
BUFFERS
(17 POSSIBLE ENTRIES)

RECEIVER SCAM BUFFER
LOAD POINTERS

(17 POSSIBLE ENTRIES)

SOFT SWITCH IN PROGRESS

-UNUSED-

OUTPUT DATA BUFFER
FOR DESTINATION 16

SCAM 2   SCAM 3   SCAM 4   SCAM 5

SCAM 2-5 ARE DATA
OUTPUT BUFFERS-
-ASSIGNED IN UNITS
OF QUARTERS

SCAM 6   SCAM 7

PARAMETER   PARAMETER
TABLE   TABLE

LEGEND:
 FIFO – FIRST IN-FIRST OUT
 SCAM – SCANNER ANSWER MEMORY

Fig. 23—Scan Memory Layout

```
        ①            ②            ③
 23 22        16  15        8   7        0
 ┌─┬──────────┐ ┌──────────────┐ ┌──────────────┐
 │P│    3E    │ │PARAMETER NUMBER│ │    DATA      │
 └─┴──────────┘ └──────────────┘ └──────────────┘


      ①    PARAMETER IDENTIFIER - THE LEFTMOST BYTE OF ALL
              PARAMETER SENDS WILL BE IDENTICAL. "P" IS THE ODD
              PERIPHERAL UNIT BUS PARITY BIT.


      ②    THE PARAMETER NUMBER IDENTIFIES WHICH OF THE 256
              POSSIBLE PARAMETERS IS BEING SUPPLIED. THIS NUMBER
              IS USED AS THE PARAMETER TABLE BYTE INDEX TO LOCATE
              STORAGE FOR THE INCLUDED ITEM OF DATA.


      ③    THE PARAMETER VALUE




      TWO BYTE PARAMETERS ARE SUPPLIED IN TWO SEND OPERATION.
      EACH IS ASSIGNED 2 PARAMETER NUMBERS.
```

Fig. 24—Structure of Peripheral Unit Controller/Data Link Application Parameter

6.41   The error message parameter consists of two bytes interpreted as a bit table in which each link is represented by the correspondingly numbered bit. If the bit is a zero, a link error message is repeated several times a second to assure its recognition by the ESS input program. This repetition is suppressed if the bit is set to a one. The original instance of the error report is not affected. This parameter can be changed at any time. The expected response to a repeated error report is setting the relevant bit in this parameter to a one. It must remain set for at least one complete audit cycle. Memory of the original error will then be erased and the parameter bit can be cleared. No reports will occur until the next error event.

B.   Destination Paraameters

6.42   The destination parameters contain information related to input and output data buffers. There are three such parameters, all controlling the allocation of the PUC/DL RAM. The destination parameters are supplied on a per destination basis, there being at most 16 sets of destination parameters. Each set contains: destination buffer length, scratch block length, and SCAM buffer length.

6.43   The destination buffer length parameter is a two byte parameter and requires two separate send operations to communicate it to the PUC/DL. It is an integer value which specifies the length (in bytes) of the send buffer to be allocated to the destination number given in the address field of the parameter (byte 2).

6.44   The SCAM buffer allocation parameter provides an output buffer for the destination specified in the address field. This parameter consists of one byte containing three 2-bit items. These items are the scanner number where the buffer is to be located, the start address of the buffer, and the length of the buffer.

6.45   The scratch block allocation parameter provides per-link areas of RAM dedicated to use protocol routines. A nonzero value in this parameter causes a block of this number of bytes to be set aside. Begin and end pointers for the scratch area are entered in the control area of the destination buffer. A scratch block parameter is entered only when the DL protocol to be used requires such an area.

C.   Data Link Basic Parameters

6.46   This category of parameter is used to specify information applicable to individual DLs but not dependent on the type of protocol to be used on that link. There are two defined parameters of this type: the protocol number and the destination number.

6.47   The protocol number parameter consists of a single byte and must be specified for each link before that link can become active. This byte contains a number telling the PUC/DL which type of DL protocol is to be used.

6.48   The destination number parameter is a single byte that states which destination buffer is to use the addressed DL.

D.   Data Link Protocol Parameters

6.49   The DL protocol parameters are not interpreted at all by the parameter input routines. They are regarded as data to be entered in the protocol parameter table allocated for the DLs specified in the parameter send. The data in these tables has meaning only to the protocol block routines. Thus the purpose of each of the parameters of this type depends on the protocol assigned to each DL.

6.50   The maximum frames parameter specifies how many information frames can be outstanding before an acknowledgment is demanded from the far-end device. This parameter is sent as one byte.

6.51   The maximum retries parameter is a single byte which specifies how many attempts the PUC/DL will make to reinitialize communication after a message has been lost or mutilated. If this number of retries fails, a DL impasse error report is sent to the ESS. The initialization attempts continue until a message is received to deactivate the DL.

6.52   The timeout parameter consists of two bytes and is presented in two separate sends. This parameter determines how long the PUC will wait for a response from the far-end device before concluding that the response is not forthcoming. This time is in 20 millisecond units.

6.53   There are two error count parameters associated with the leaky bucket error rate mea-

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36

surement. Each is two-byte value having two independent addresses. The threshold is the value of the accumulated count which will generate an error report. The increment is the amount by which the count is increased whenever an error is detected. The accumulated count is decremented whenever a transmission is successful.

E. Parameter Table

6.54 The operational parameters for the PUC/DL are stored in a visible parameter table to facilitate auditing by the ESS. This table consists of the entire contents of SCAMs 6 and 7. To locate a particular parameter, use the value of bits 8 through 15 in the word that would be sent to the PUC/DL to specify that parameter. This number is the byte offset from the beginning of SCAM 6. To access the table, a row address must be supplied. That address is the above value shifted right one position, with rows bigger than 63 being interpreted as in memory 7 and reduced by 64. The contents of the table entries are the lower byte of the parameter exactly as it was presented by the ESS when its value was last changed. Derived parameter values will also appear in the table. These are quantities such as the destination number of a DL when it was presented in a reconfiguration instruction.

7. REFERENCES

7.01 The following documents provide further information in related areas.

DOCUMENT	SUBJECT
231-115-501	Office Alarms
231-037-021	DCT Description
231-090-154	ETS Feature
231-090-152	DCT Feature
231-090-062	PUC/DL Feature
231-090-153	RSS Feature
231-037-022	RSS Interface and Maintenance Considerations
231-105-302	Procedures for Taking Equipment Out of Service

DOCUMENT	SUBJECT
231-050-000	DCT (TOP)
231-050-027	PUC/DL Maintenance (TOP)
231-037-023	ETN Interface And Maintenance Considerations
231-050-015	PUC/DCT Maintenance (TOP)
PK-1A473	PUC Diagnostic Description—No. 1 ESS
SD-1A477-01	PUC/DCT Schematic
SD-1A478-01	PUC/DL Schematic
SD-1A479-01	PUC Power and Alarm Schematic

8. ABBREVIATIONS

8.01 The following abbreviations are used in this section.

ASM	Auxiliary Scan Memory
ASW	All Seems Well
BWM	Broadcast Warning Message
CC	Central Control
CCIS	Common Channel Interoffice Signaling
CCU	Combined Channel Unit
CP	Central Processor
CPD	Central Pulse Distributor
CPU	Controller Processor Unit
DCT	Digital Carrier Trunk
DCU	Digroup Controller Unit
DIF	Data Input FIFO
DIFC	Data Input FIFO Controller

DL	Data Link	PSR	Pulsing State Register
DMA	Direct Memory Access	PUAB	Peripheral Unit Address Bus
DR	Digroup Register	PUC	Peripheral Unit Controller
EPROM	Erasable Programmable Read Only Memory	PUP	Peripheral Unit Parity
ESS	Electronic Switching System	RAM	Random Access Memory
ETS	Electronic Tandem Switching	ROM	Read Only Memory
FIFO	First In First Out	SCAB	Scanner Answer Bus
HCM	Hardcore Matcher	SCAM	Scanner Answer Memory
I/O	Input/Output	SCAMC	Scanner Answer Memory Controller
IOD	Input-Output Decoder	SCANS	Software Change Administration And Notification System
IOM	Input-Output Matcher	SP	Signal Processor
LIU	Line Interface Unit	TOP	Task Oriented Practice
MEN	Mode and Enable	TR	Trunk Register
POB	Peripheral Order Buffer	TTY	Teletypewriter
PROMUS	Prompt Remotely Operated Memory Update System	UTS	Universal Trunk Scanner.

21.4 MHz FM Demodulator

Overview

This is a project for an add−on FM demodulator for a radio receiver, or other piece of test equipment, equipped with a 21.4 MHz IF output. This demodulator was designed specifically for use with a HP8569B RF spectrum analyzer and may require additional pre−amplification if used on other gear.

The FM demodulator is based around a standard Motorola MC3361 low−power narrowband FM IF chip. The MC3361 is no longer in production, but you can salvage them from older analog 49 MHz cordless phones and baby monitors. The 455 kHz quadrature coil and IF filter for the MC3361 can also be salvaged from the same circuit which you got the MC3361 from.

The MC3361 will also require a 20.945 MHz crystal (or 21.855 MHz) to convert the 21.4 MHz input down to the standard 455 kHz IF signal. These 20.945 MHz crystals will need to be salvaged from a FM two−way or ham radio which also operated with a 21.4 MHz IF. You may have to poke around your local hamfests and buy up a bunch of radios before finding one with the correct 20.945 MHz crystal. Be sure to note the value of the loading capacitors on the crystal for proper oscillation. These values may need to be tweaked a bit if the crystal doesn't oscillate.

An optional squelch circuit will also be added to the FM demodulator circuit. This squelch circuit will act just like the standard squelch control in a radio, only passing audio when the incoming RF signal reaches a certain level to avoid having to listen to "noise." The squelch level is set via a panel−mounted 10 kohm potentiometer. The squelch circuit is a little buggy and will still pass a little bit of audio noise when "squelched," but it's not a bit deal and I just left it.

The demodulated audio output from the MC3361 is then sent to a National LM380 2.5 watt audio amplifier to power an internal speaker. A standard National LM386 can be used if you only want to drive a pair of headphones or a lower power speaker.

The RF input to the MC3361 is via a simple LC network (3 µH / 18 pF) to match the incoming 50 ohms to the MC3361's impedance of 3300 ohms. You may wish to add a little bit of amplification on the RF input, if your application requires it. The MC3361 has a fairly low intercept point, so don't add too much gain or you'll just get distortion and intermodulation products.

An optional **Filter Select** switch will allow the bypassing of the narrowband Murata 455 kHz IF filter with a 0.1 µF capacitor. This is for when you need to listen to wider bandwidth FM signals. The overall sensitivity of the circuit will be reduced in this mode, which is common.

Review the datasheet for the Motorola MC3361 before constructing this circuit to get an idea of what the components do. Monitor the 20.945 MHz crystal's oscillation via a high−impedance oscilloscope and adjust the values of the two loading capacitors if it doesn't oscillate on startup. The quadrature coil can also be slighty tuned for minimum distortion when viewing the demodulated audio output on an oscilloscope.

Pictures & Construction Notes
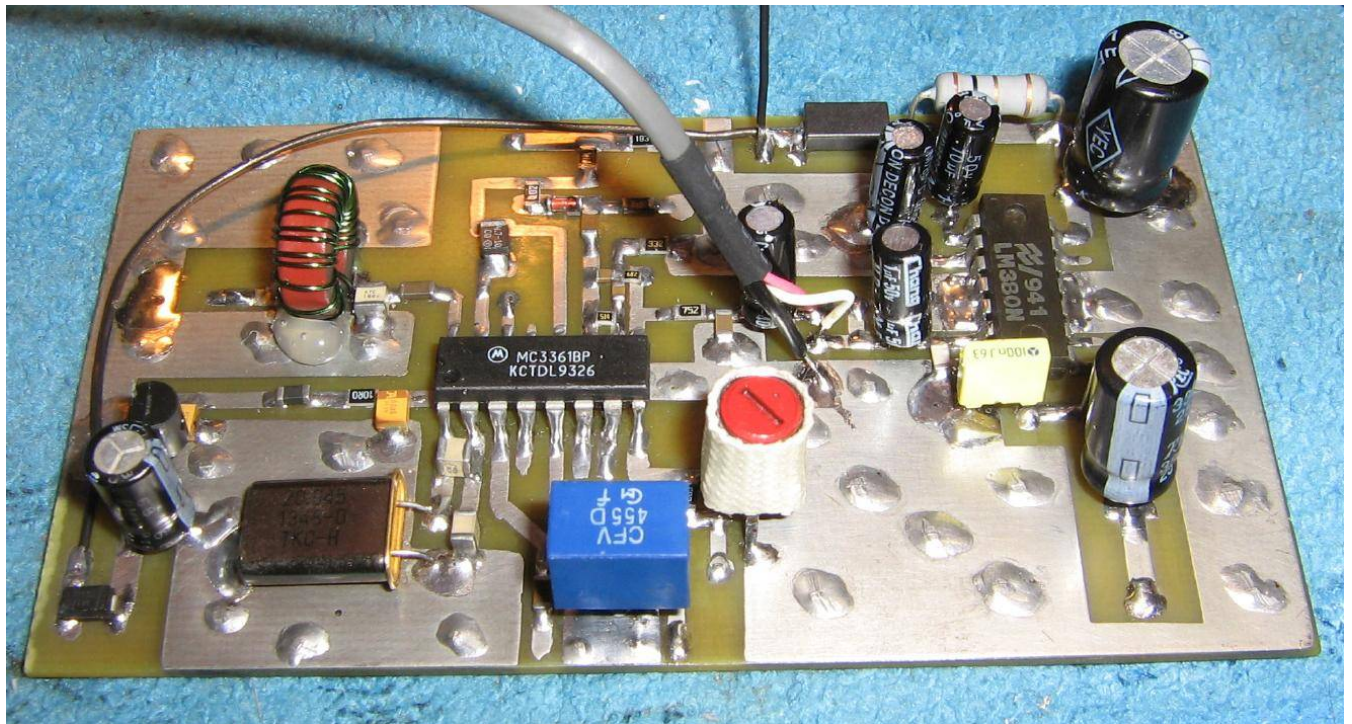
Overview of the 21.3 MHz FM Demodulator circuit.

The 21.4 MHz 50 ohm RF input is on the upper−left via the LC network feeding the MC3361.

The blue square thing is a Murata 455 kHz IF filter with a 6 dB bandwidth of +/− 10 kHz. Other similar IF filters will also work.
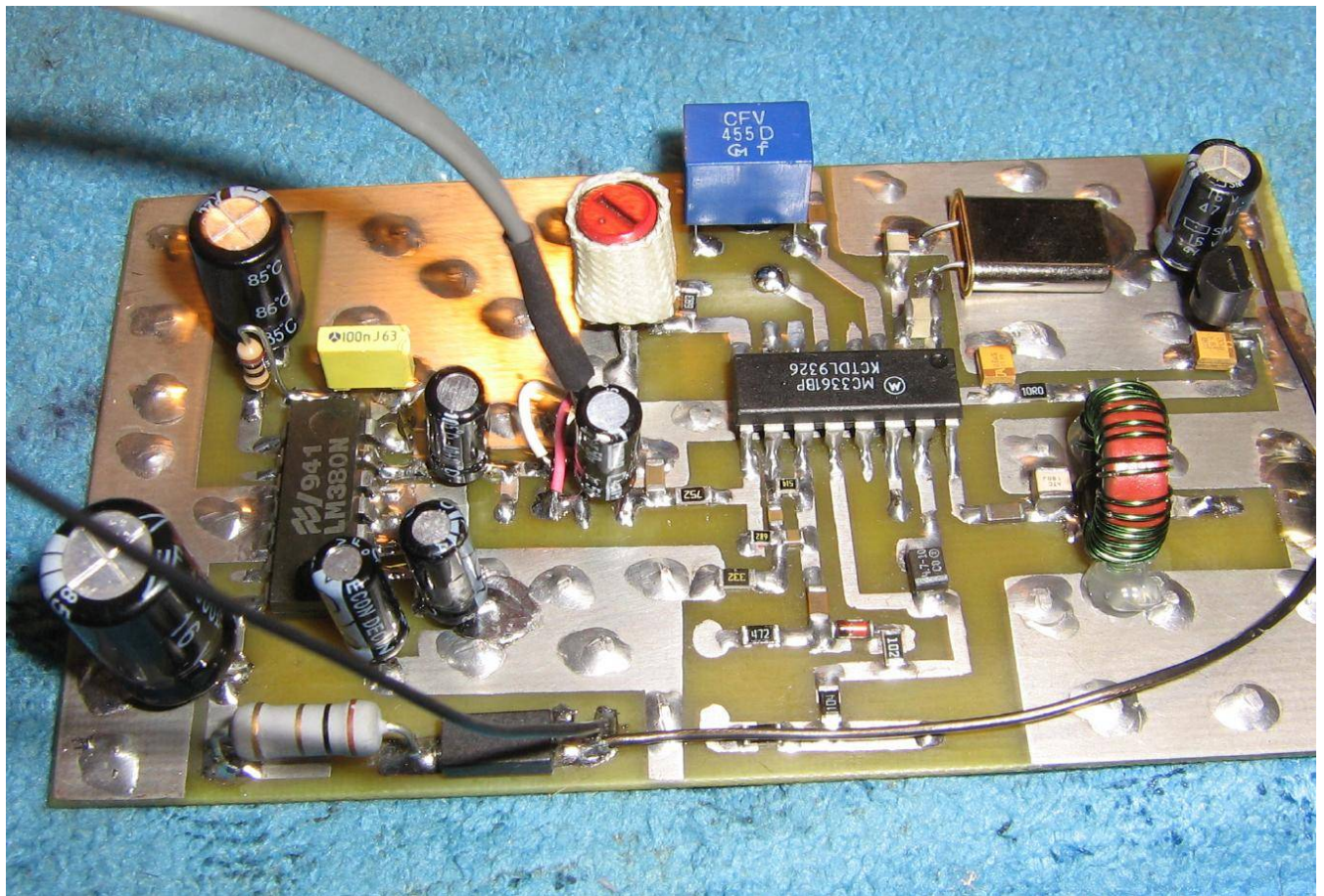
The variable core is the 455 kHz quadrature coil.

The silver rectangle laying down next the MC3361 is the 20.945 MHz crystal.

A 78L05 voltage regulator along the left−side powers the MC3361.

The LM380 audio power amplifier is along the right−side.

Alternate view.

The large ferrite bead and 1 ohm power resistor help to de−Q the LM380's power line to prevent oscillation.
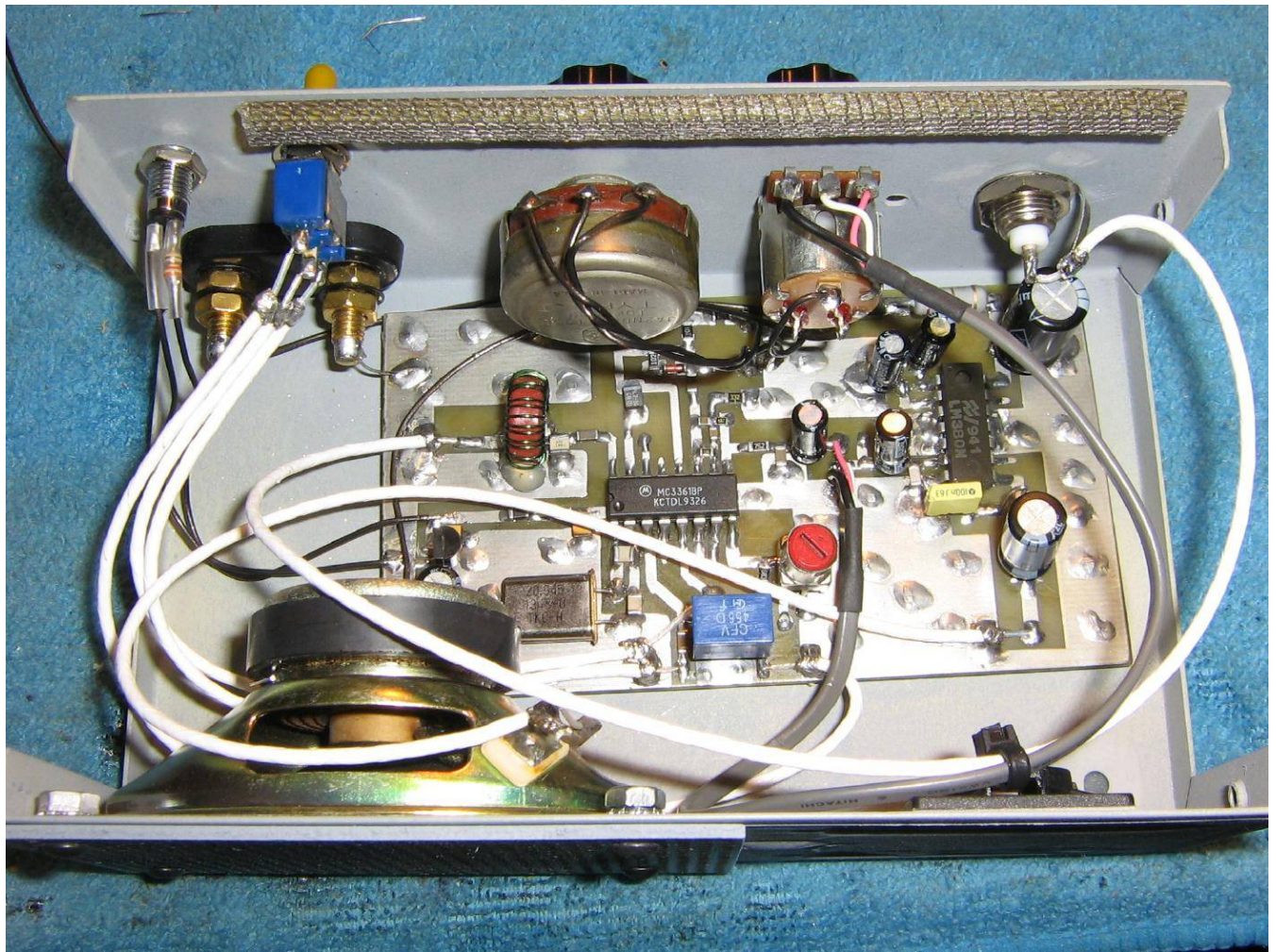
Mounting the circuit board in an old printer switch case.

+12 VDC power input is via the banana jacks on the upper−left. A power−indicating LED and the **Filter Select** switch are above it.

The 10 kohm squelch potentiometer is in the middle of the panel with the 10 kohm power/volume potentiometer next to it.

The BNC jack is for the 21.4 MHz IF input.

A 5 watt / 8 ohm speaker was mounting internally inside the case. You'll need to cut out the rear of the case to avoid obstructing the audio output from the speaker.
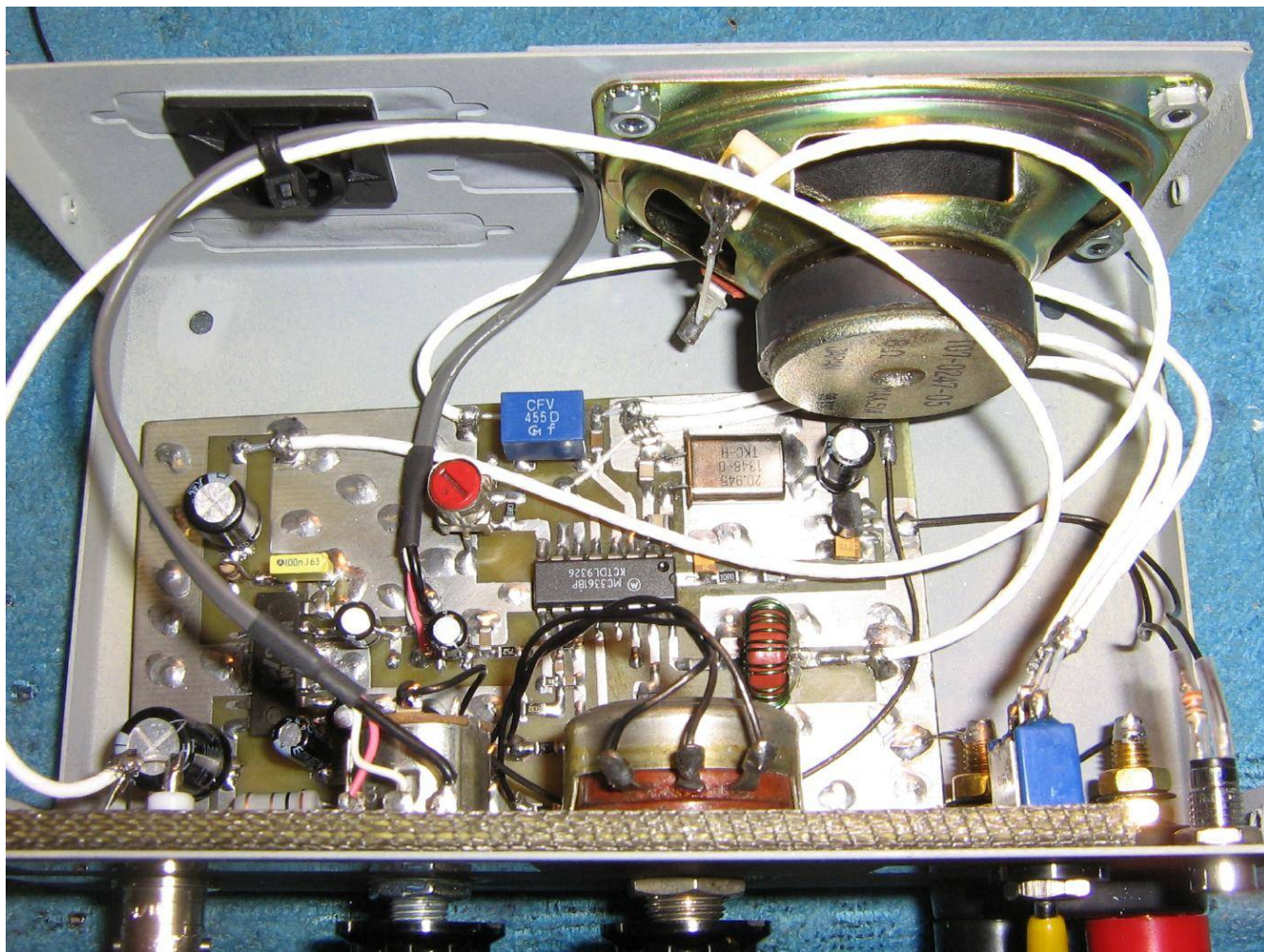
Alternate internal view.

The white wires are coaxial lines for the **Filter Select** and speaker connection.

Using coaxial cables for those connections is optional, but it will reduce the chance of receiving interference.
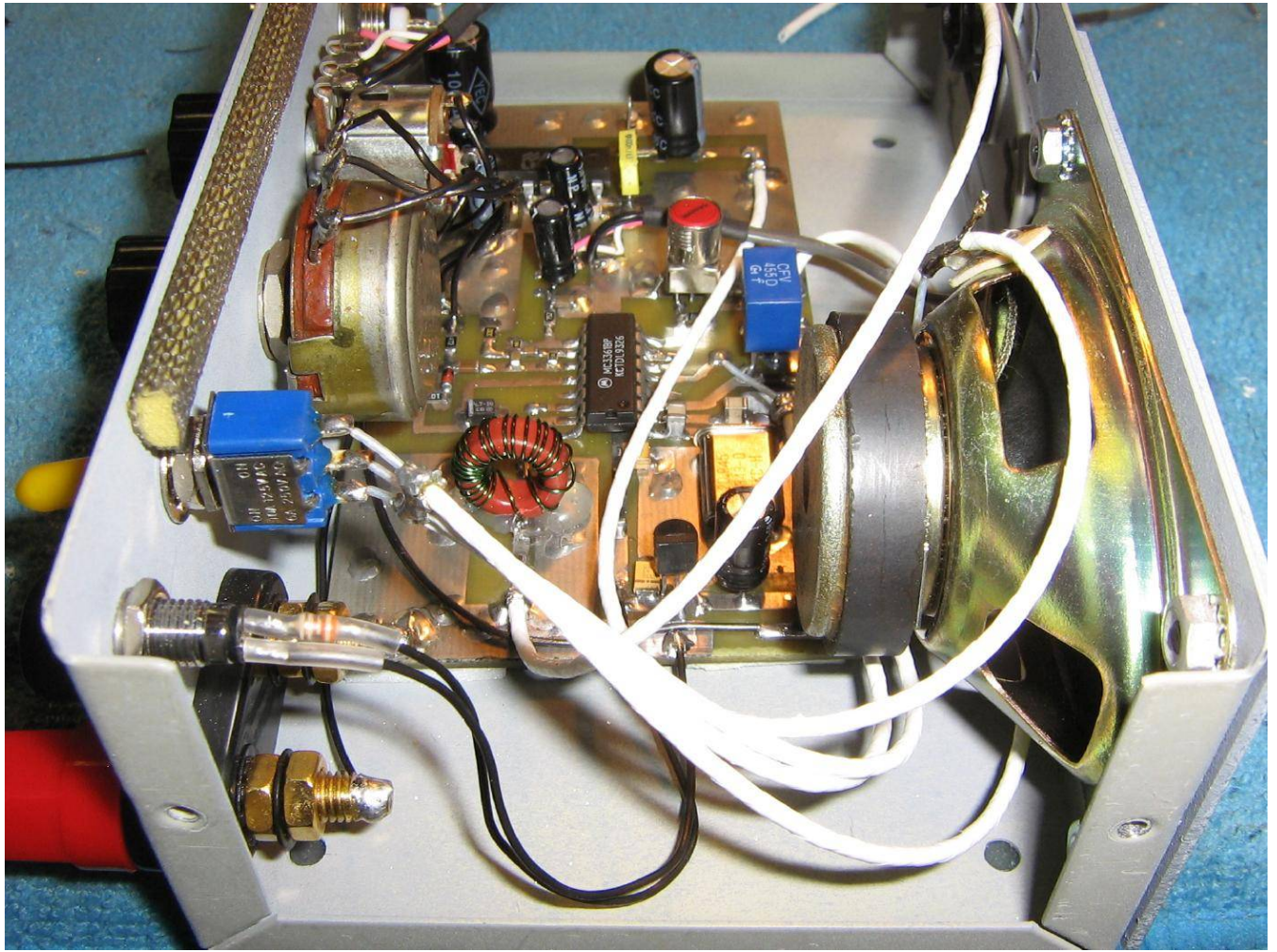
Internal side−view showing the installation of the rectangular 5 watt / 8 ohm speaker.

Use the LM386 instead of the LM380 if you only want to power a 1 watt or smaller speaker or headphones.
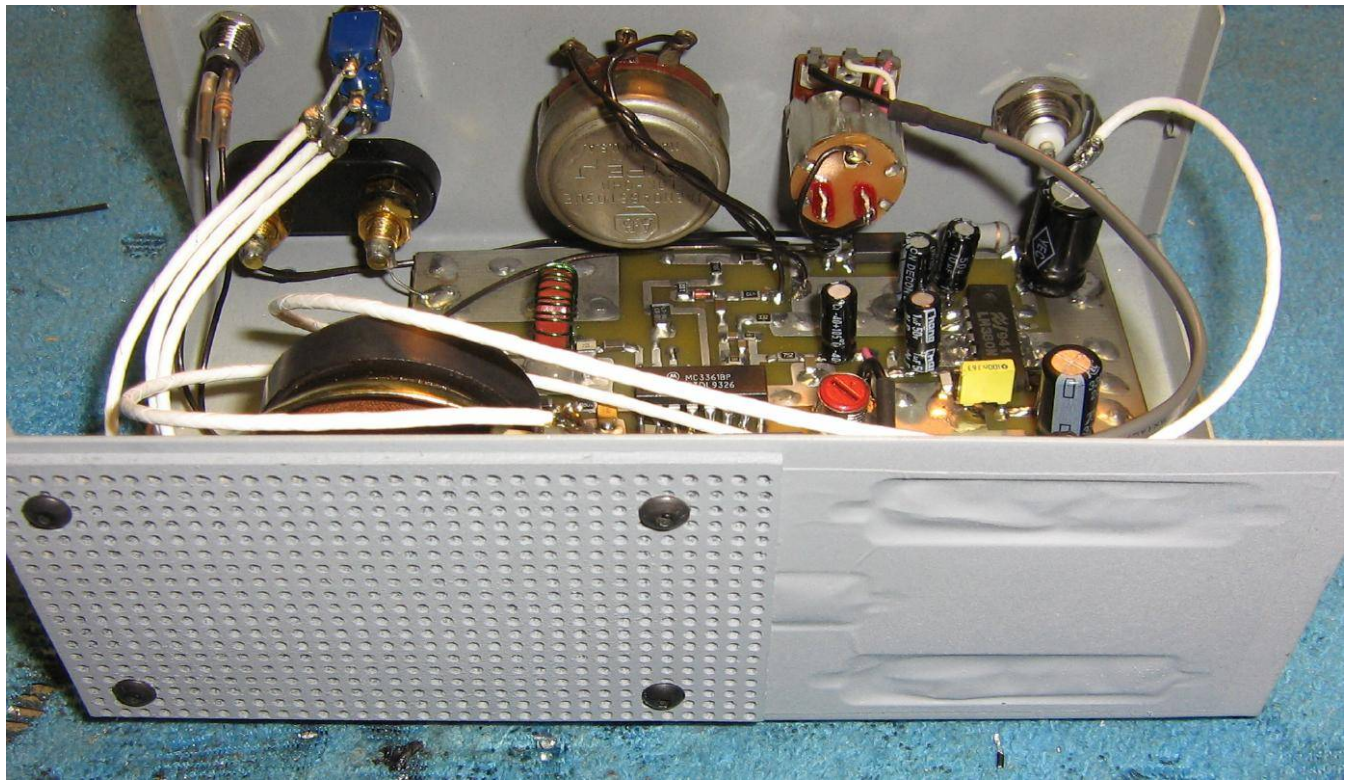
Completed rear−panel overview.

A piece of perfboard was added over the speaker's opening to act as a grill.

Completed front–panel overview.

The **21.4 MHz Input** is via the BNC jack on the left.

The **Power/Volume** control is the potentiometer next to that.

The **Squelch** control is the potentiometer in the center.

Banana jacks on the lower–right provide the +12 VDC power input. The current draw can peak around 1+ amps at high audio volume, so take this into account.

Above the banana jacks is a power–indicating LED and the **Filter Select** switch.

21.4 MHz FM Demodulator

Audio Amplifier

+12 VDC

Ferrite Bead

1 Ω / 3W

1000 µF

LM380

10 µF

10 µF

10 µF

1 µF NP

100 pF

NC

NC

Large groundplane for heatsink.

330 µF

10 Ω 1/4W

0.1 µF

Speaker 8Ω / 5W

Mute To MC3361 pin 14

A

Volume 10 kΩ Panel-Mount

1 µF NP

0.01 µF

7.5 kΩ

6.8 kΩ

3.3 kΩ

Squelch 10 kΩ Panel-Mount

18 kΩ

4.7 kΩ

1N914

1 kΩ

100 kΩ

4.7 µF

0.1 µF

1000 pF

1000 pF

470 kΩ

Motorola MC3361

NC

455 kHz Quadrature Coil L = 1 mH variable C = 120 pF

68 kΩ

2x 0.1 µF

Filter Select Narrow/Wide SPDT / Panel-Mount

Murata CFV455D *(Bottom View)*

0.1 µF

47 pF

22 pF

455 kHz IF Filter

0.01 µF

L1

18 pF

0.1 µF

20.945 MHz

Tweak loading caps for proper oscillation.

21.4 MHz IF Input

10 µF

10 Ω

Ferrite Bead

+5 VDC

L1 = 25 turns #26 on T-50-2 powered-iron toroid. Approx. 3 µH

NP = Non-Polarized

Homebrew "Firefly" Infrared Beacon

Overview

The military often uses flashing infrared beacons to mark perimeters, identify targets, outline landing zones, or to mark friendly forces. Since these beacons operate at infrared wavelengths, they are not visible to the human eye but are easily viewable with standard light–amplification night vision gear.

The most common of these beacons is made by KERIF Night Vision (NSN: 5855–01–438–4588) and is called the "Phoenix Jr." or "Firefly." They have two main versions, with one running off a standard 9 volt battery and the other using a CR123 battery.

The Firefly uses three infrared LEDs operating at the 880 nm wavelength. The flash rate is 1.3 seconds and the flash duration is around 20 milliseconds. This flash rate was chosen to minimize confusion with small–arms fire.

The beacons offer an omnidirectional optical coverage zone of 240° x 360°.

The funny thing is, these infrared beacons are covered via International Traffic in Arms Regulations (ITAR) and sales are restricted by the U.S. State Department to law enforcement or government agencies only!

Yep, three infrared LEDs, a battery, a 555 timer, a couple transistors, resistors & capacitors – **all of which are available from Radio Shack** – are considered "restricted" by the U.S. government.

So... Here's how to make your own!

Pictures & Construction Notes
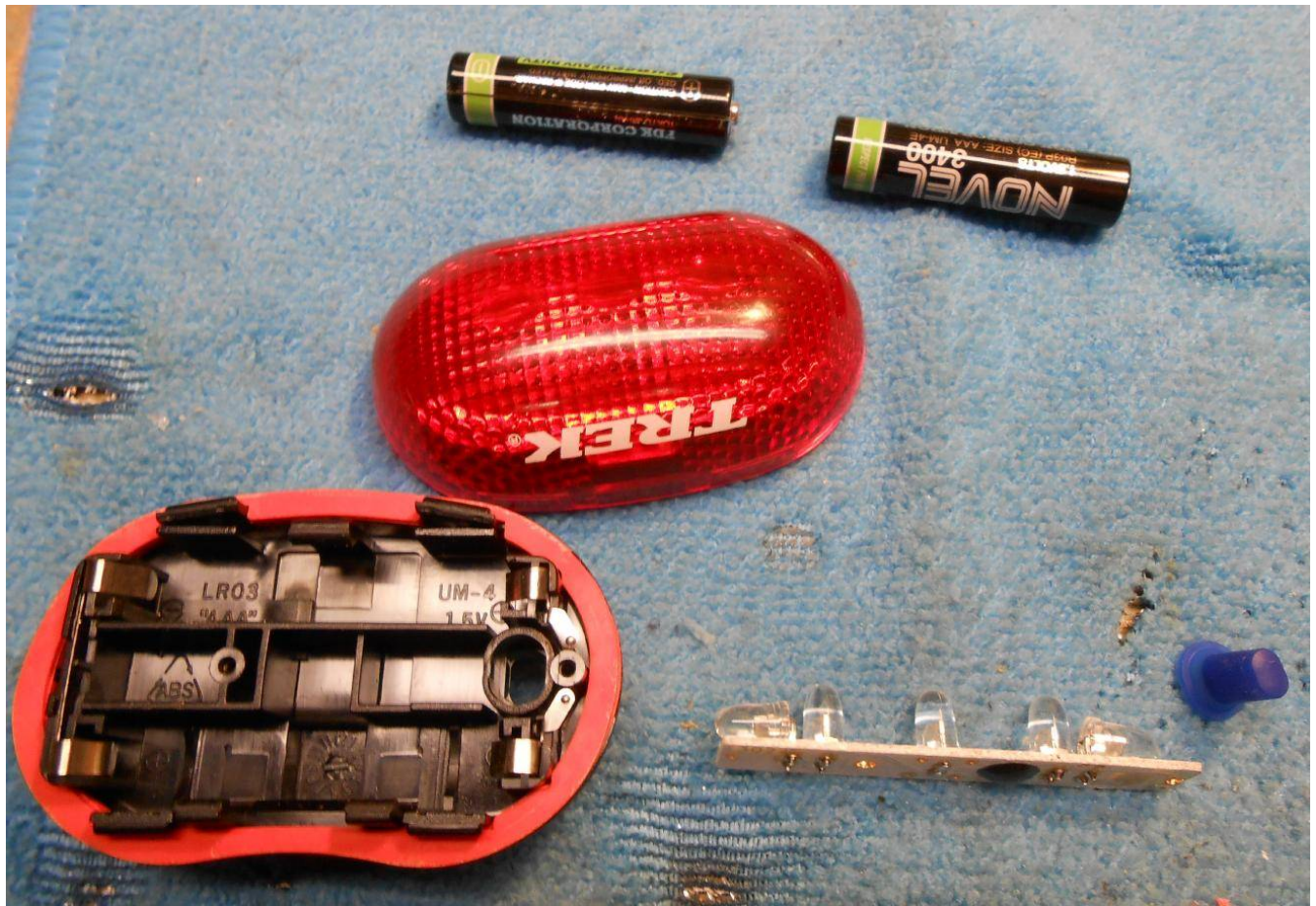
First, you'll need a flashing red LED taillight from your local bicycle shop. There are a whole bunch of different models available, but make sure it has a selectable "flashing" mode.

Take the tailight apart and count the number of LEDs inside it. The Trek Flare model used for this article had five red LEDs – three facing forward and two facing off to either side.
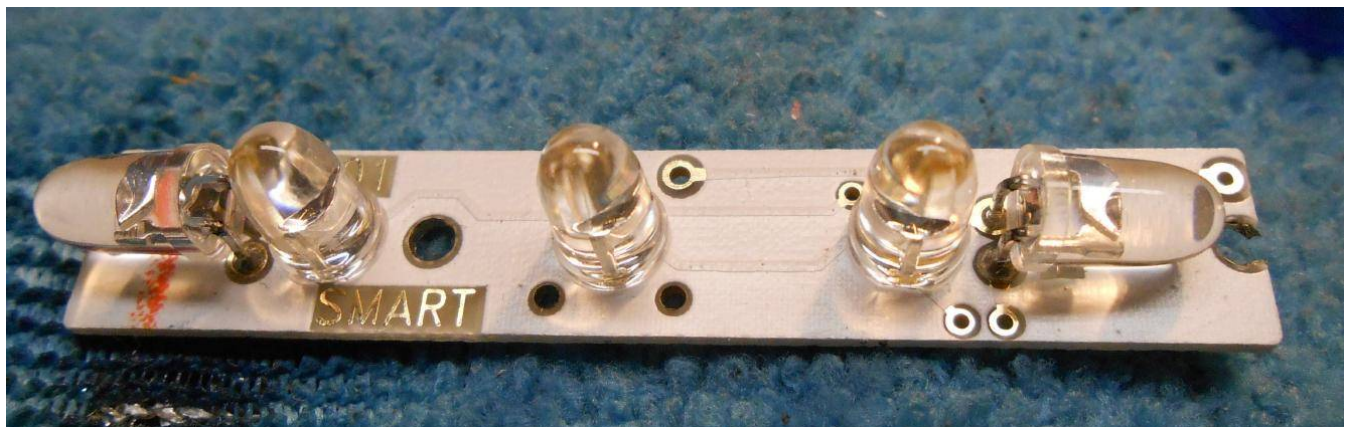
Closeup view of the stock red LEDs in the flashing Trek taillight.
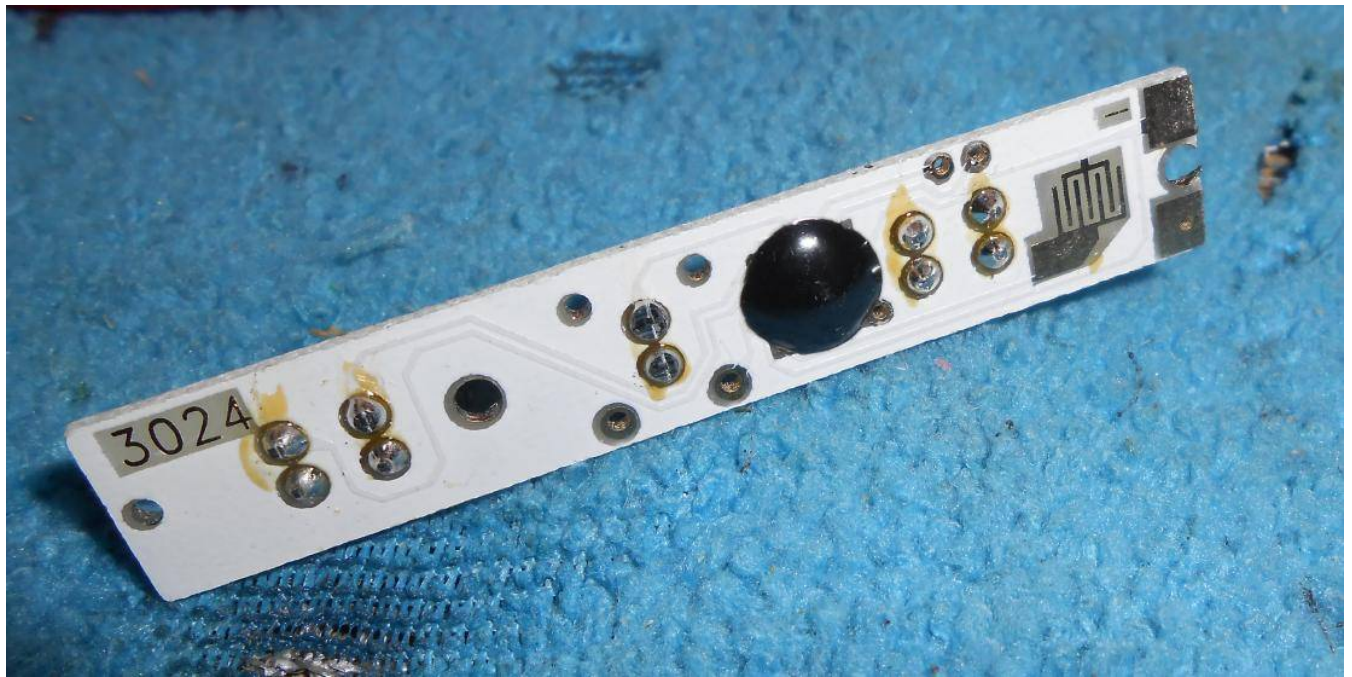
Bottom view of the circuit board.

There's not much too it and you can't really adjust the flashing rate. Most of these bicycle taillight beacons tend to flash a little faster than the Fireflys.

The +3 VDC power from the two "AAA" batteries is applied via those pads on the upper−right.

Go to Radio Shack and pick up some infrared LEDs (Part #: 276–0142). These come paired with a phototransistor, but the infrared emitting LED (850 nm) will be the one with the tinted lens package.

Another source of infrared emitter LEDs (940 nm, usually) is from old TV/VCR remote controls.
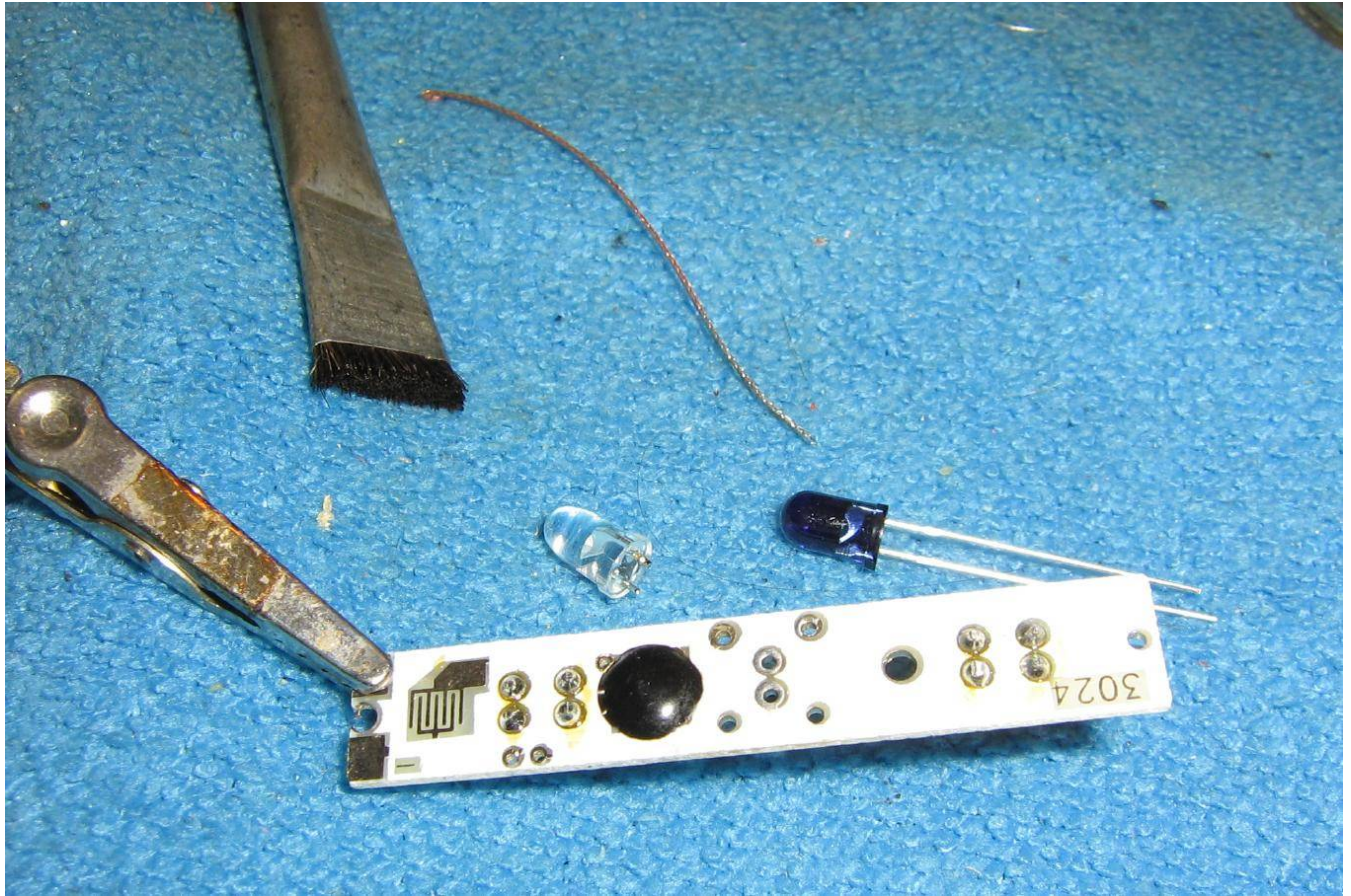
Unsolder the stock LEDs in the taillight, being sure to note the "flat" side of the LED's package. That will be the cathode or negative lead.

You should double–check the polarity of the LEDs with a multimeter, as the "flat" side isn't always the cathode on some of the cheaper import LEDs.
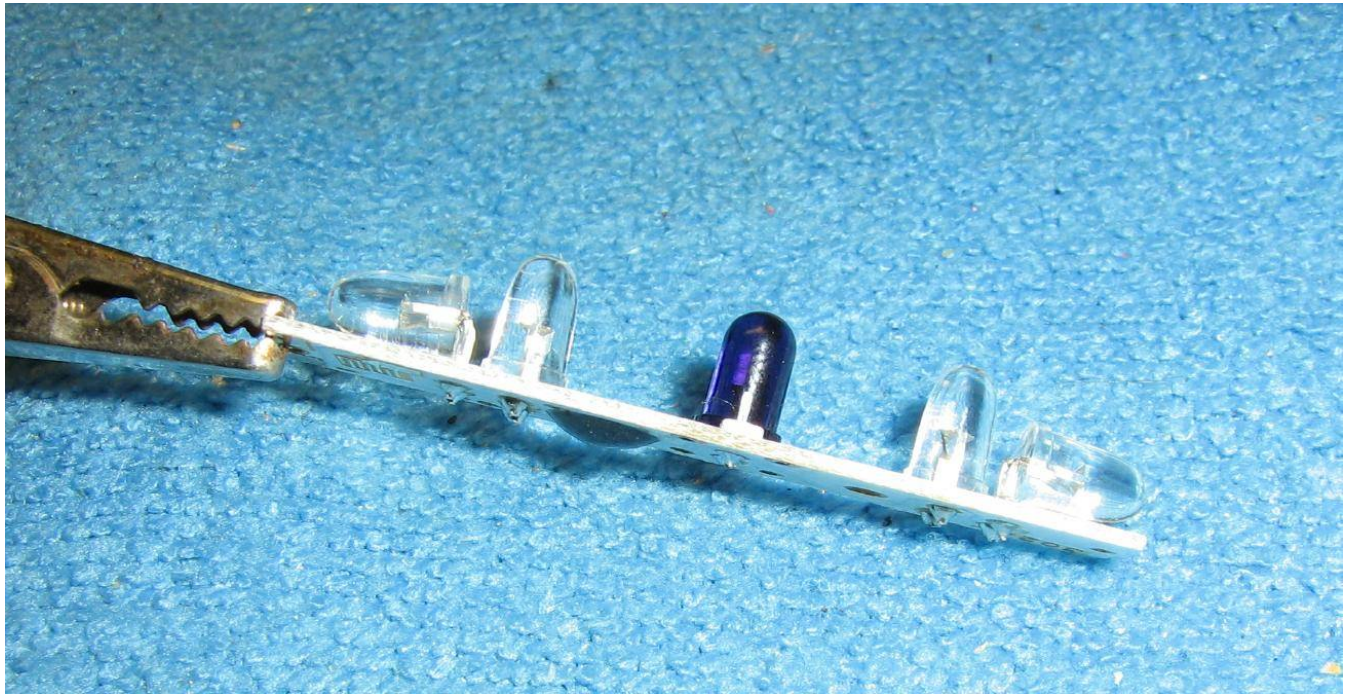
Install the new infrared LEDs, again noting the position of the "flat" side of the LED.
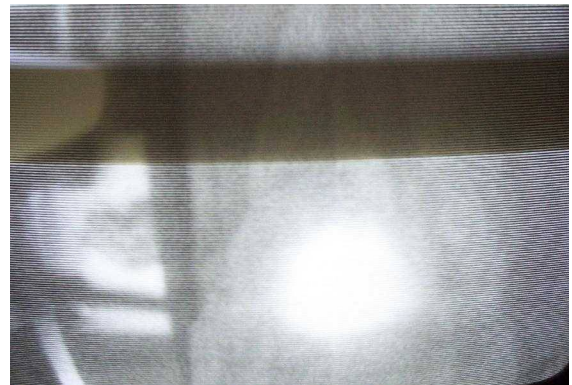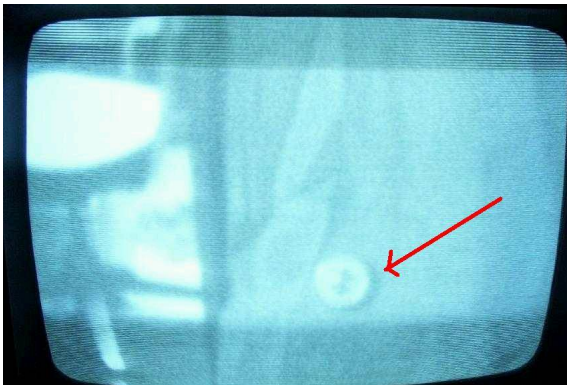
Reinstall the batteries and test the unit by viewing it with a video or cell phone camera (which may require removing the internal infrared blocking filter), or by using your own night vision gear.

The infrared LEDs should *NOT* be visible to the human eye but should be readily viewable with your night vision setup.

The Only Type of Gun Control Which Works

Any Questions?

Editorial and Rants
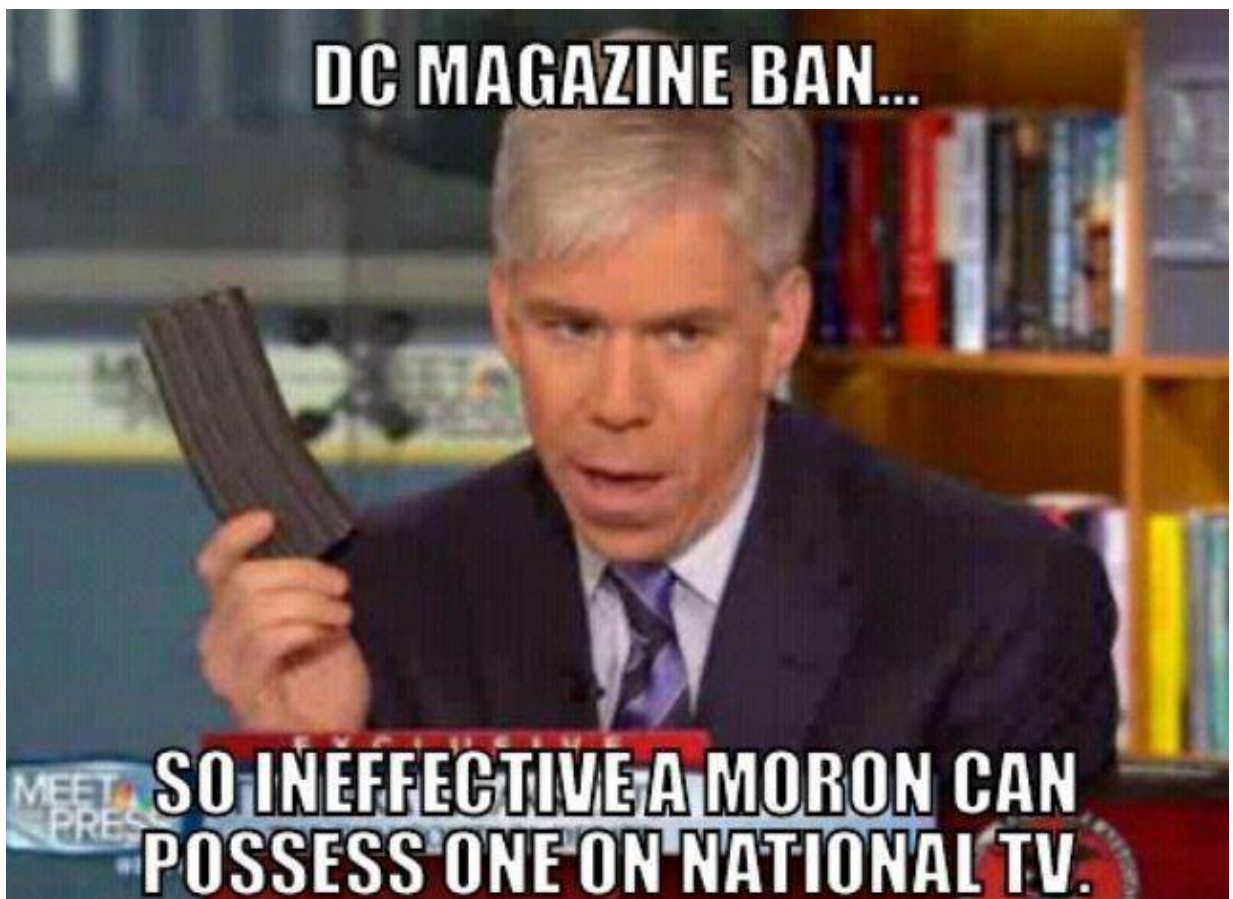
DC MAGAZINE BAN... SO INEFFECTIVE A MORON CAN POSSESS ONE ON NATIONAL TV.

Send them back to Africa! LOL! Now why can't White countries do the same thing? Doesn't Israel like racial "diversity and multiculturalism?" Gotta love the hypocrisy...

Netanyahu Ready for 'Stage 2' in Expelling Migrants

December 24, 2012 – *From: jpost.com*

by Yoni Dayan and Ben Hartman

Prime Minister Binyamin Netanyahu on Monday signaled he was ready to begin repatriating African migrants, which he termed the "second stage" in the effort to clear Israel of illegal infiltrators.

"We have succeeded in blocking the entry of infiltrators from Africa to Israel," Netanyahu said at the start of a discussion he convened on the issue. "After having faced the threat of the entry of hundreds of thousands, this month, not one infiltrator entered Israel's cities."

The prime minister said that after workers complete construction of the the security fence being built along Israel's southern border next month, Israel will start working to send migrants already in Israel back to their home countries. "Now we are moving on to the second stage, that of repatriating the infiltrators who are already here."

Netanyahu appointed a special representative, Hagai Hadas, to oversee the repatriation of "tens of thousands of infiltrators" to their countries of origin. There are currently an estimated 60,000 migrants residing in Israel, mostly originating from Sudan and Eritrea. Thousands of migrants are being held in detention facilities in the South, with Israel's "infiltrator law" enabling authorities to imprison without trial for up to three years anyone who has entered the country illegally.

Though many politicians have campaigned heavily on the issue of repatriating African migrants, the move has been largely hampered by legal caveats. On Hanukkah, right–wing MKs Michael Ben–Ari and Arieh Eldad held a candle–lighting ceremony in south Tel Aviv to issue a call to expel all African migrants from Israel. They labeled the event "banishing the darkness."

The Association for Civil Rights in Israel (ACRI) issued a scathing attack on the government policies pertaining to African migrants earlier this month, charging that, inter alia, the State was refusing to examine asylum requests and was instead treating all migrants as illegal.

Sigal Rozen, the public policy coordinator for the Hotline for Migrant Workers said that she doesn't think that the move will happen and that is mostly just a political statement made by Netanyahu ahead of the January elections.

"We don't think it will happen because we know it's impossible and we also don't think he'll stoop that low, to deport thousands of refugees back to the countries they fled."

Rozen also took note of the timing of the message, which came on Christmas Eve, saying that most of the Eritreans in Israel, who make up the majority of the migrants in Israel, are Christian.

Rozen added "He's always saying stuff like this, this is not the first time. We'll have to see if it's something more serious or just an attempt to win votes from the far–right."

Murder & Non-Negligent Manslaughter Victim,Suspect and Arrestee Race Ethnicity
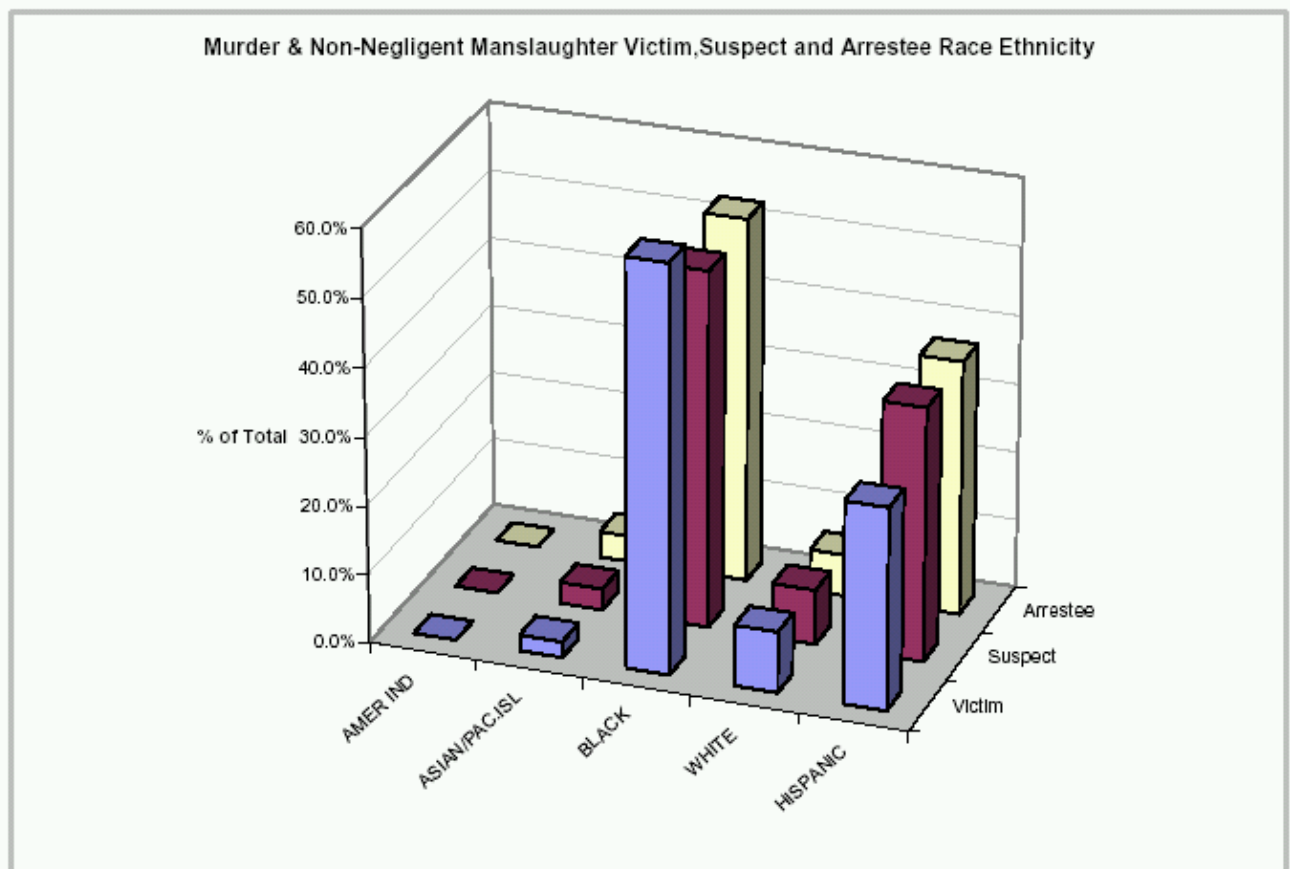
Murder and Non-Negligent Manslaughter Victim, Suspect, Arrestee Race/Ethnicity

	Victim	Suspect	Arrestee
AMER IND	0.0%	0.0%	0.0%
ASIAN/PAC.ISL	2.3%	3.1%	3.8%
BLACK	59.3%	51.9%	53.1%
WHITE	8.9%	8.0%	6.1%
HISPANIC	29.4%	37.0%	37.1%
Total Complaints/Arrests	215	162	213
Known Race Ethnicity	214	162	213
% of Incidents With Race/Eth. Known	99.5%	100.0%	100.0%

Minority Control – Not Gun Control

90% of murders in Eric Corley's New York City are caused by Blacks and Hispanics (Mestizos).

(nyc.gov/html/nypd/downloads/pdf/analysis_and_planning/enforcement_report_1st_6_months_2011.pdf)
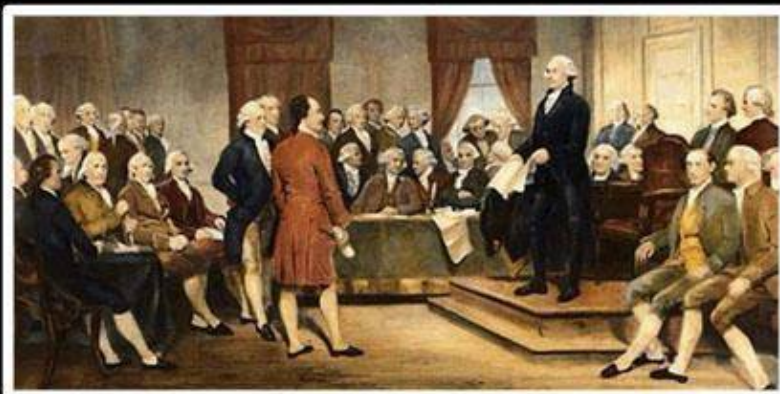
This is the publisher of the *Journal News* in New York who thinks it's O.K. to publish an online map which lists the names and addresses of *legally* registered gun owners.

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Feel free to share her information as freely as she sees fit to share others'.